MODEL TTS 59C/CR
UNIVERSAL SENDER

SERVICE MANUAL

Northeast Electronics Instruction Manual
A0059-30-601 Issue 1 May 1980

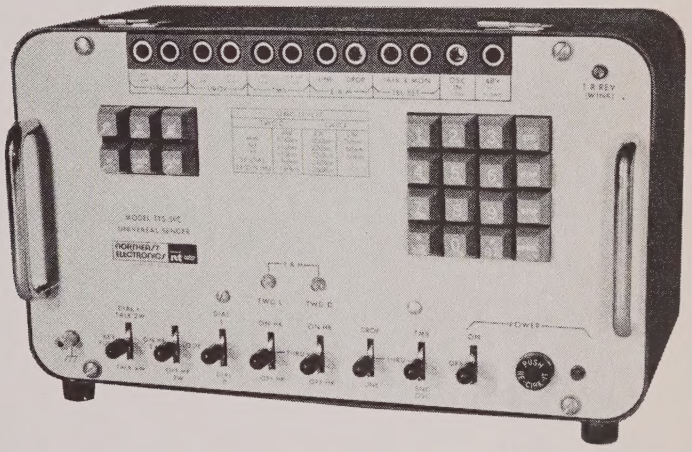
northern telecom

BUONTEMPO
PROVISION

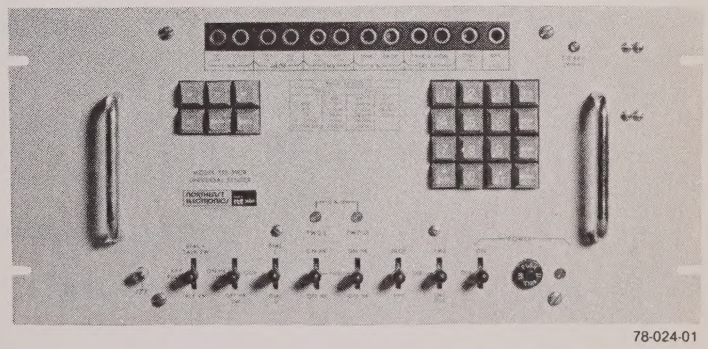
CONTROLLED
DOCUMENT

MODEL TTS 59C/CR
UNIVERSAL SENDER

SERVICE MANUAL



78-015-01



78-024-01

Northeast Electronics Instruction Manual
A0059-30-601 Issue 1 May 1980

northern telecom

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_08132

TABLE OF CONTENTS

SECTION	TITLE	PAGE
1	**GENERAL DESCRIPTION**	1–1
	1.3 Supervisory Signaling	1–1
	1.4 Addressing Signaling	1–1
	1.6 Typical Applications	1–1
	1.8 Input Power	1–1
2	**SPECIFICATIONS**	2–1
3	**INSTALLATION**	3–1
	3.2 Controls, Indicators And Jacks	3–1
4	**OPERATION**	4–1
	4.2 General Block Description	4–1
	4.9 Functional Description	4–2
	4.11 Dial Pulse Generation	4–2
	4.16 SF Supervision	4–5
	4.21 SF Address Signaling	4–5
	4.24 MF And TT Signaling	4–5
	4.28 E&M Switching	4–6
	4.34 LINE/DROP, SEND/RECEIVE Switching	4–6
	4.37 Test Signal Switching	4–6
	4.41 Measurement Switching	4–7
	4.43 Monitor Switching	4–7
	4.46 Detailed Circuit Descriptions	4–7
	4.50 Dial Pulse Generator	4–7
	4.54 Clocks	4–8
	4.57 Tone Generator Control	4–8
	4.61 Tone Generator Sine ROM	4–11
	4.63 E&M Send Circuit	4–11
	4.65 E&M Receive Circuit	4–13
5	**MAINTENANCE AND CALIBRATION**	5–1
6	**DIAGRAMS**	6–1
7	**ELECTRONICS PARTS LIST**	7–1

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
3–1	Operating Controls	3–1
4–1	General Block Description	4–3
4–2	Power Distribution Diagram	4–8
4–3	Dial Pulse Timing For Loop And E&M Addressing	4–9
4–4	Tone Generator Control Timing	4–10
4–5	Sine ROM Output For A Single Input	4–12
6–1	Functional Block Diagram	6–2
6–2	Dial Pad Assembly A1 Parts Location Diagram	6–4
6–3	Dial Pad Assembly A1 Schematic Diagram	6–5
6–4	Keypad A1A2 And Dial Pulse Generator A1A2 Parts Location Diagram	6–6
6–5	Keypad A1A1 And Dial Pulse Generator A1A2 Schematic Diagram	6–7

LIST OF ILLUSTRATIONS (Cont'd).

FIGURE	TITLE	PAGE
6–6	Tone Generator A1A3 Parts Location Diagram	6–8
6–7	Tone Generator A1A3 Schematic Diagram	6–9
6–8	E&M Board A2 Parts Location Diagram	6–10
6–9	E&M Board A2 Schematic Diagram	6–11
6–10	Relay Board A3 Parts Location Diagram	6–12
6–11	Relay Board A3 Schematic Diagram	6–13
6–12	Interconnection Diagram	6–14
6–13	Overall Assembly Diagram	6–15
6–14	Sub Panel Assembly Parts Location Diagram	6–16
6–15	Jack Block Assembly	6–17
6–16	Top Unit Assembly Diagram	6–18

LIST OF TABLES

TABLE	TITLE	PAGE
2–1	Models TTS 59C And TTS 59CR Specifications	2–1
2–2	MF And TT Frequencies	2–2
3–1	Front Panel Access Jacks	3–3
3–2	Front Panel Lever Switches	3–5
3–3	Addressing Controls	3–7
3–4	Front Panel Indicators	3–8
4–1	E&M Supervision Selections	4–11
4–2	Monitor Thresholds	4–13
4–3	E-Lead Monitor Thresholds	4–13
4–4	M-Lead Switch S7 Factory Settings	4–13
4–5	E-Lead Switch S8 Factory Settings	4–13
7–1	Overall Parts List	7–1
7–2	Keypad A1 Parts List	7–1
7–3	Dial Pulse Generator A1A2 Parts List	7–2
7–4	Tone Generator A1A3 Parts List	7–3
7–5	E&M Board A2 Parts List	7–4
7–6	Relay Board A3 Parts List	7–5
7–7	Sub Panel Assembly Parts List	7–6
7–8	Jack Block Assembly Parts List	7–6

SECTION 1

GENERAL DESCRIPTION

1.1 This manual describes the Northeast Electronics Models TTS 59C and TTS 59CR Universal Senders. These test sets generate supervisory and address signals used in testing various types of telephone circuits. The sets also include access and switching features that permit both sending and receiving. Provisions are also made for use of external oscillators and transmission measurement sets (TMS). The combination of the TTS 59C and a two-way TMS such as the Northeast Electronics Model TTS 44 provides the means for accessing and, if necessary, communicating with the far end during transmission tests. Test lines are routinely accessed in use of the test sets.

1.2 The Model TTS 59C is a portable unit, enclosed by a metal housing and a protective cover. The TTS 59CR is rack-mounted and is identical to the TTS 59C in all other respects. Except for obvious physical differences, any statement made about the TTS 59C also applies to the TTS 59CR. A row of jacks across the upper edge of the front panel accepts 310-type plugs for patching to test bays, a power source, and auxiliary instruments. A row of lever switches across the bottom of the panel controls routing of supervisory, address, and information signals. A six-button array on the left side of the panel selects the addressing mode. The sixteen-button keypad allows selection of numerals and multi-frequency (MF) functions. Indicators show the state of loop and E&M circuits.

1.3 **Supervisory Signaling** toward either the line or drop is possible in three modes.

- Loop
- E&M
- SF

The E&M monitor and indicator circuit includes a settable threshold to assure that indications of supervisory states result from E&M circuit voltages exceeding a minimum acceptable level.

1.4 **Addressing Signaling** toward either the line or drop is possible in five modes.

- Dial pulse
- E&M pulsing
- SF
- MF
- TT (Touch Tone®)

The MF addressing mode can be used with any supervisory mode. The TT pairs can also be produced to local loops and test private switching networks. Ten pulses per second are set for dial pulse, E&M, and SF. Percent break is 61 percent. The E&M sending circuit can provide any combination of open, ground, and protected battery in on-hook and off-hook conditions. Type I, II, and III are easily accomodated.

1.5 Communication can be established with either the line or drop on two- or four-wire circuits. The test set accepts a type 52A, or equivalent, telephone headset for this purpose. The headset is also used to monitor in-band signals sent to the circuit under test by the unit. Two-way transmission test signals are connected through the set. Pads in the test set are switched to inject appropriate levels into line and drop two- or four-wire circuits.

1.6 **TYPICAL APPLICATIONS.**

1.7 The Model TTS 59C Universal Sender has capabilities needed for:

- acceptance testing of new installations,
- routine testing of in-service installations, and
- sectionalizing.

The test set interfaces with trunk circuits through VF patch bays and patching jack bays such as two-, four-, and six-wire patch bays. The many sending modes, including the programmable E&M mode, make the set usable with most trunk types.

1.8 **INPUT POWER**

1.9 The TTS 59C operates from -48 V CO battery at a maximum load current of 0.6 Ampere. Power is applied to the unit through a 310-type jack. The power switch, circuit breaker, and power indicator are clustered at the lower right corner of the front panel.

® Registered trade mark of A. T. & T.

SECTION 2

SPECIFICATIONS

2.1 Table 2—1 lists the specifications of the Models TTS 59C and TTS 59CR Universal Senders.

Table 2—1. Models TTS 59C and TTS 59CR Specifications.

DIAL PULSE GENERATOR	
Frequency	10 ± 1pps
Percent break	61 ± 6%
Interdigit time	780 ± 50 m sec
Digit storage capacity (DP and SF modes only)	up to 16 digits
IN-BAND TONE SIGNALING	
Frequencies	Standard MF, TT, plus 2400 Hz and 2600 Hz SF (See Table 2—2)
Frequency accuracy	± 1%
Total harmonic distortion	≤ 2.5 %
Duty cycle	39 ± 2%

OUTPUT LEVELS

OUTPUT TYPE	LEVEL		
	DROP SEND 4W	LINE S/R S4W	
		4W	2W
MW (+7dBm at J2 or J7)	+7dBm	−16dBm	0dBm
MF, TT	+1dBm	−22dBm	−6dBm
SF (DIAL)	−1dBm	−24dBm	
SF (ON HK)	−13dBm	−36dBm	

OUTPUT LEVEL ACCURACY ± 1.0dB

E&M MONITOR INDICATORS

LINE OR DROP E&M JACKS		INDICATORS	
		TWD.L	TWD.D
Tip	Ring		
−12.8 ± 1V	Ground	On	Off
Ground	−12.8 ± 1V	Off	On

Table 2—1 (Cont'd).

E&M SENDING

E&M SWITCH		E&M JACK
OFF HK	TWD. L	−48V resistive LINE (ring)
ON HK	TWD. L	GROUND LINE (ring)
OFF HK	TWD. D	GROUND DROP (tip)
ON HK	TWD.D	OPEN DROP (tip)

OUTPUT IMPEDANCE	600 ± 42 Ω
INPUT IMPEDANCE	600 ± 42 Ω
BRIDGING IMPEDANCE	100 k ohms, minimum
POWER REQUIREMENT	
Voltage Range	−46 to −53 V
Current Range	300 to 500 mA
DIMENSIONS (TTS 59C)	14 in w x 8¾ in h x 8 in d (35.6 cm x 22.2 cm x 20.3 cm)
WEIGHT (TTS 59C)	13 lb. (5.9 kg)
DIMENSIONS (TTS 59CR)	19 in. w x 8¾ in. h x 8 in. d (48.3 cm x 22.2 cm x 20.3 cm)
WEIGHT (TTS 59CR)	11.5 lb. (5.2 kg.)
OPERATING TEMPERATURE RANGE	0°C to +50°C (+32°F to + 122°F)
OPERATING RELATIVE HUMIDITY	0 to 95% non-condensing

Table 2—2. MF And TT Frequencies

DIGIT	MF	TT
1	700, 900	697, 1209
2	700, 1100	697, 1336
3	900, 1100	697, 1447
4	700, 1300	770, 1209
5	900, 1300	770, 1336
6	1100, 1300	770, 1477
7	700, 1500	852, 1209
8	900, 1500	852, 1336
9	1100, 1500	852, 1477
0	1300, 1500	941, 1336
*,KP	1100, 1700	941, 1209
#,ST	1500, 1700	941, 1477
STP	900, 1700	— — — —
ST2P	1300, 1700	— — — —
ST3P	700, 1700	— — — —

SECTION 3

CONTROLS, INDICATORS, AND JACKS

3.1 This section contains a complete functional description of all controls, indicators, and jacks for the Model TTS 59C Universal Sender.

3.2 **CONTROLS, INDICATORS, AND JACKS.**

3.3 All front panel controls, indicators, and jacks are identified on Figure 3—1. Table 3—1 lists the twelve 310-type access jacks located at the top center of the panel. The table is arranged to show the application of each jack and the internal incoming and outgoing connections made to each jack by the various switching combinations. Table 3—2 lists seven of the eight lever switches. This table identifies the application of each switch, describes the influence of each switch on incoming and outgoing signals, and identifies all related switching requirements for each switch position. The address mode controls included in the six-button array and the sixteen-button dial keypad are described in Table 3—3. This table includes applications and related switching requirements. Table 3—4 describes the front panel indicators.

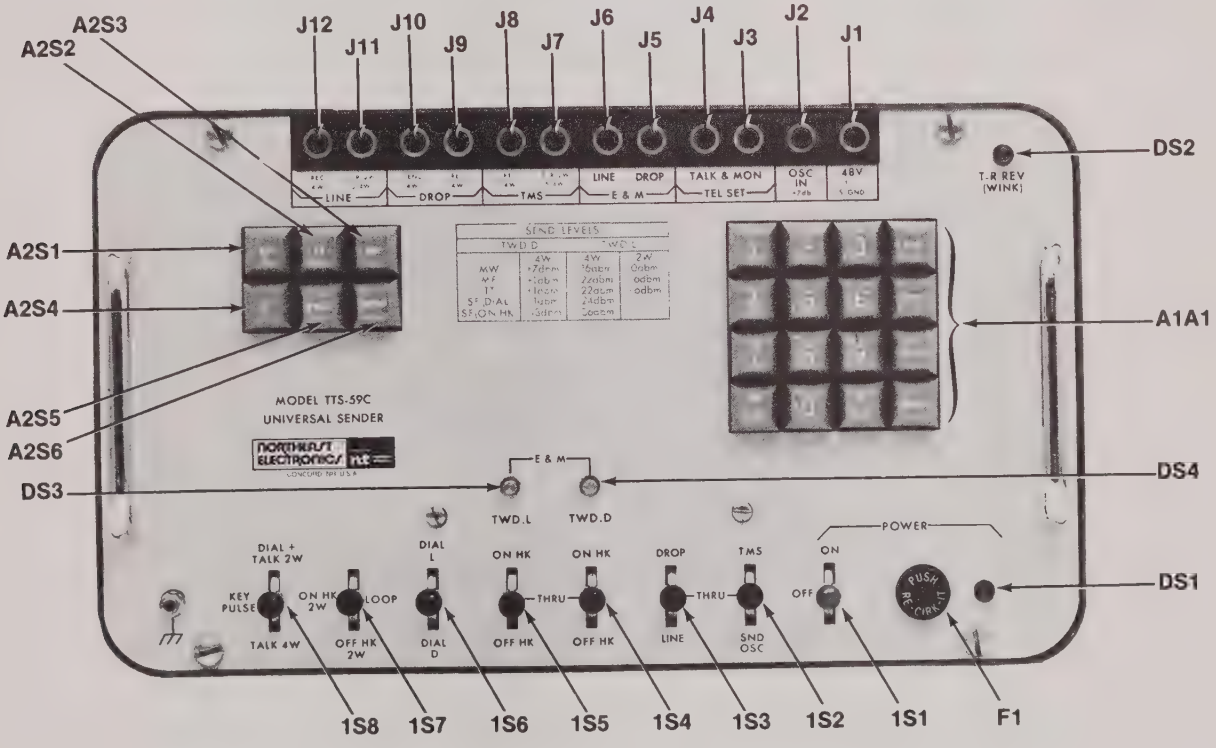


Figure 3—1. Model TTS 59C Operating Controls.

Table 3—1. Model TTS 59C Front Panel Access Jacks.

REF DES	NOMENCLATURE	INCOMING		TEST SET APPLICATION(S)	OUTGOING	
		EXTERNAL SOURCE	SWITCHED TO		SWITCHED FROM	EXTERNAL DESTINATION
J1	48V, T = −, S = GN	Office or accessory supply	Test set circuits	All	Not applicable	Not applicable
J2	OSC IN +7 dB	Test oscillator; (appropriate levels delivered to circuit under test with +7 dBm input)	J11 or J10 (SEND) and J3/J4 (MON)	Transmission path loss and gain-slope tests	Not applicable	Not applicable
J3/J4	TEL SET TALK & MON	Transmitter of type 52A or equivalent telephone headset	J11 or J10 (SEND)	Sending: communication with far end Receiving: a. communication with far end b. through-connected VF circuit under test Monitor: a. external TMS or oscillator signal b. In-band supervisory and address signals	a. J12 or J9 (REC) b. J12 or J9 (REC) c. J2 (OSC) or J7 (TMS) d. Tone generator	Receiver of type 52A or equivalent telephone headset
J5	E&M DROP	Drop M lead	Line M lead (with TWD. L OFF HK/THRU/ON HK switch S5 at THRU) and TWD. D indicator DS4	All E&M operations	Line E lead (with TWD.D OFF HK/THRU/ON HK switch S4 at THRU) or E&M supervision and pulsing circuit (with TWD. L switch S5 at ON HK or OFF HK)	Drop E lead
J6	E&M LINE	Line E lead	Drop E lead (with TWD.D OFF HK/THRU/ON HK switch S4 at THRU) and TWD. L indicator DS3	All E&M operations	Drop M lead (with TWD. L OFF/HK/THRU/ON HK switch S5 at THRU) or E&M supervision and pulsing circuit (with TWD. D switch S4 at ON HK or OFF HK)	Line M lead
J7	TMS S/R 2W S4W (SEND/RECEIVE TWO-WIRE, SEND FOUR-WIRE; given as TMS SEND in text)	TMS instrument	J11 or J10 (SEND) and J3/J4 (MON)	Transmission loss and gain-slope tests, especially as implemented with TMS sets having send and receive capabilities	J11 (receiving two-wire)	TMS instrument
J8	TMS REC 4W	Not applicable	Not applicable	Transmission loss and gain-slope tests, especially as implemented with TMS sets having send and receive capabilities	J12 or J9 (REC)	TMS instrument
J9	DROP REC 4W	Drop four-wire VF circuit	a. J11 (SEND) and J3/J4 (MON) b. 600-ohm termination c. 600-ohm termination and J3/J4 (MON) d. J3/J4 (MONITOR) e. J8 (MEASURE) and J3/J4 (MON)	a. Through-connected, monitored circuit under test b. Any operation toward the line c. Sending in-band supervisory or address signals d. Sending external oscillator signal or communicating e. Transmission loss and gain-slope test (receiving TMS signals)	Not applicable	Not applicable

Table 3—1. (Cont'd).

REF DES	NOMENCLATURE	INCOMING		TEST SET APPLICATION(S)	OUTGOING	
		EXTERNAL SOURCE	SWITCHED TO		SWITCHED FROM	EXTERNAL DESTINATION
J10	DROP SEND 4W	Not applicable	Not applicable	a. Through-connected circuit under test b. Any operation toward the line c. Sending in-band supervisory or address signals d. Talking on four-wire drop circuit under test e. Transmission loss and gain-slope tests (sending oscillator signal) f. Transmission loss and gain-slope tests (sending TMS signal)	a. J12 (REC) b. 600-ohm termination c. Tone generator (SF, TT, MF) d. J3/J4 (TRANSMITTER) e. J2 (OSC) f. J7 (TMS)	Drop four-wire VF circuit
J11 On 2W	LINE S/R 2W S4W (SEND/ RECEIVE TWO-WIRE, SEND FOUR-WIRE, given as LINE SEND in text)	Line two-wire VF circuit	a. J9 (REC) and J3/J4 (MON) b. J7 (TMS) and J3/J4 (MON) c. J3/J4 (MON)	a. Through-connected, monitored two-wire circuit under test b. Transmission loss and gain-slope tests c. Communication on two-wire circuit d. Transmission loss and gain-slope tests (sending oscillator signal) e. Sending supervisory and address signals	a. J7 (TMS) b. J3/J4 (MON) c. J2 (OSC) d. Supervisory circuit and dial pulse generator	Line two-wire VF circuit
J11	Not applicable	Not applicable	Not applicable	a. Through-connected four-wire circuit under test b. Any operation toward the drop c. Sending in-band supervisory or address signals d. Talking on four-wire line circuit under test e. Transmission loss and gain-slope tests (sending TMS signal) f. Transmission loss and gain-slope tests (sending oscillator signal)	a. J9 (REC) b. 600-ohm termination c. Tone generator (SF, TT, MF) d. J3/J4 (MON) e. J7 (TMS) f. J2 (OSC)	Line four-wire VF circuit
J12	LINE REC 4W (Jack includes switch that inserts 16 dB-pad when plug inserted and 1S3 in LINE position)	Line four-wire VF circuit	a. J10 (SEND) and J3/J4 (MON) b. 600-ohm termination c. 600-ohm termination and J3/J4 (MON) d. J3/J4 (MON) e. J8 (TMS) and J3/J4 (MON)	a. Through-connected, monitored circuit under test b. Any operation toward the drop c. Sending in-band supervisory or address signals d. Sending external oscillator signal or communicating e. Transmission loss and gain-slope tests (receiving TMS signal)	Not applicable	Not applicable

Table 3—2. Model TTS 59C Front Panel Lever Switches.

REF DES	NOMENCLATURE	POSITION	INFLUENCE ON LINE OR DROP SIGNALS		ASSOCIATED SWITCHING REQUIREMENTS	APPLICATION
			FROM CIRCUIT UNDER TEST TO TEST SET	FROM TEST SET TO CIRCUIT UNDER TEST		
1S2	TMS/THRU/SND/OSC	TMS	Connects LINE REC 4W jack J12 or DROP REC 4W jack J9 to TMS REC 4W jack J8; connects LINE S/R 2W S4W jack J11 to TMS S/R 2W S4W jack J7.	Connects TMS S/R 2W S4W jack J7 to DROP SEND 4W jack J10 or LINE S/R 2W S4W jack J11.	Select LINE or DROP (1S3); select KP (1S3) to monitor outgoing TMS tone and select REC jack (J9 or J12).	Two- and four-wire transmission loss and gain-slope tests.
		THRU	Permits termination of selected REC jack (J9 or J12) while sending in-band supervisory and address signals.	Permits connection of transmitter, dial or in-band signaling to SEND jack J11 or J10.	Select LINE or DROP (1S3).	See 1S8.
		SEND OSC	None.	Connects OSC IN +7 dB jack J2 to selected SEND jack (J11 or J10).	Select LINE or DROP (1S3); select KP (1S3) to monitor outgoing tone and selected REC jack (J12 or J9).	Transmission loss and gain-slope tests.
1S3	DROP/THRU/LINE	LINE	Connects LINE REC 4W jack J12 to monitor and measurement circuits (four-wire tests); connects LINE S/R 2W, S4W to monitor and measurement circuits (two-wire tests). Terminates J9 (600 ohms).	Connects external circuit (such as TMS) to monitor and LINE S/R 2W S4W jack J11; inserts 7-dB pad into send path (except during two-wire dial pulsing); allows insertion of 16-dB pad (23 dB total) during four-wire line tests. See J12. Terminates J10 (600 ohms).	Select KP (1S8); to monitor non-talk signal.	VF operations toward the line.
		THRU	Connects LINE REC 4W jack J12 to DROP SEND 4W jack J10 and monitor; connects DROP REC 4W jack J9 to LINE S/R 2W S4W jack J11 and monitor.	See column 4; external circuit disconnected.	Select KP (1S8) to monitor REC jacks (J12 and J9).	Pass uniterrupted circuit through test set.
		DROP	Connects DROP REC 4W jack J9 to monitor and measurement circuits; terminates J12 (600 ohms).	Connects external circuit (such as TMS) to monitor and DROP SEND 4W jack J10.	Select KP (1S8) to monitor non-talk signal.	VF operation toward the drop.
1S4	TWD. D ON HK/THRU/ OFF HK	ON HK	None.	Sends on-hook to drop on E lead jack J5.	None.	E&M operations toward the drop.
		THRU	Connects line E lead jack J6 to drop E lead jack J5.	See column 4.	1S6 must be in CENTER position.	E&M operations toward the line; pass uninterrupted circuit under test E lead through test set.
		OFF HK	None.	Sends off-hook or address signals toward the drop on E lead jack J5.	Select DIAL D (1S6) to address.	E&M operations toward the drop.
1S5	TWD. L ON HK/THRU/ OFF HK	ON HK	None.	Sends on-hook to line on M lead jack J6.	None.	E&M operations toward the line.
		THRU	Connects drop M lead jack J5 to line M lead jack J6.	See column 4.	1S6 must be in CENTER position.	E&M operations toward the drop; pass uninterrupted circuit under test M lead through test set.
		OFF HK	None.	Sends off-hook or address signals toward the line on M lead jack J6.	Select DIAL L (1S6) to address.	E&M operations toward the line.

Table 3—2. (Cont'd).

REF DES	NOMENCLATURE	POSITION	INFLUENCE ON LINE OR DROP SIGNALS		ASSSOCIATED SWITCHING REQUIREMENTS	APPLICATION
			FROM CIRCUIT UNDER TEST TO TEST	FROM TEST SET TO CIRCUIT UNDER TEST		
1S6	DIAL D/CENTER/DIAL L	DIAL L	None.	Connects dial pulses to line M lead jack J6 through 1S6.	Select TWD. L OFF HK (1S5).	E&M operations toward the line.
		CENTER	None.	Disables E&M signaling.	None.	Through-connected circuit under test E&M circuit.
		DIAL D	None.	Connects dial pulses to drop E lead jack J5 through 1S4.	Select TWD. D OFF HK (1S4).	E&M operations toward the drop.
1S7	LOOP ON HK 2W/OFF HK 2W	ON HK 2W	None.	Sets two-wire on-hook condition.	Select DIAL + TALK 2W (1S8).	Beginning and final condition for line two-wire operations.
		OFF HK 2W	Connects LINE S/R 2W S4W jack J11 to T-R REV (WINK) indicator (DS2).	Sends "off-hook" to LINE S/R 2W S4W (J11, connects dial pulses.	Select LINE (1S3) and DIAL + TALK 2W (1S8).	Signaling two-wire line circuit.
1S8	DIAL + TALK 2W/KEY PULSE/TALK 4W	DIAL + TALK 2W	Connects LINE S/R 2W S4W jack J11 to monitor.	Connects transmitter to LINE S/R 2W S4W jack J11 and monitor.	Select THRU (1S2) and LINE (1S3).	Communicate on two-wire circuit.
		KEY PULSE (KP)	Enables monitor channels A and B; see Table 4—5.	Connects in-band supervisory and address signals to LINE S/R 2W S4W (J11) or DROP SEND 4W (J10).	Select THRU (1S2) and LINE or Drop (1S5).	Sending in-band supervisory and address signals.
		TALK 4W	Connects LINE REC 4W jack J12 or DROP REC 4W jack J9 to monitor.	Connects transmitter to LINE S/R 2W S4W jack J11 or DROP SEND 4W jack J10.	Select THRU (1S2) and LINE or DROP (1S3).	Communicate on four-wire circuit.

Table 3—3. Model TTS 59C Addressing Controls.

REF DES	NOMEN-CLATURE	PURPOSE	APPLICATION(S)	ASSOCIATED SWITCHING REQUIREMENTS
A2S1	DP	When latched, enables 10-pps dial pulse generator.	a. Loop dial pulsing. b. E&M pulsing. c. SF signaling.	a. Select loop OFF HK 2W; use keypad numerals. b. Select DIAL L (or D) and set E&M L (or D) at OFF HK; use keypad numerals. c. Select KP (not TALK; 1S8), set 1S2 at THRU; see A2S4.
A2S2	TT	Enables standard Touch-Tone® signaling, latching.	TT address and TT information functions.	Select KP (not TALK; 1S8), set 1S2 at THRU; use keypad numerals.
A2S3	MF	When latched, enables standard two-of-five multi-frequency signaling.	MF addressing.	Select KP (not TALK; 1S8), set 1S2 at THRU; use keypad numerals.
A2S4	SF	When latched, enables single frequency signal in conjuction with 2400 and 2600.	a. SF on-hook supervision. b. SF signaling.	a. Latch 2400 or 2600; select KP (not TALK; 1S8), set 1S2 at THRU. b. Latch 2400 or 2600, latch DIAL; see also entry c under A2S1.
A2S5	2400	When latched, selects 2400 Hz for SF tone.	SF supervisory and address signals.	Latch SF; see also A2S4.
A2S6	2600	When latched, selects 2600 Hz for SF tone.	SF supervisory and address signals.	Latch SF; see also A2S4.
None	0-9	Numeral buttons.	All addressing modes.	Latch DIAL, TT or MF.
None	* KP	Keypulse...prepares receiving circuit for digits.	Precedes dialing digits in MF signaling.	None.
None	# ST	Start pulse...indicates all digits have been sent.	Follows dialing digits in MF signaling.	None.
None	STP, ST2P, ST3P	TSPS and other functions.	MF information.	None.
None	REDIAL	Causes last-entered DP or SF address to be retransmitted once each time button is pressed when dial pulsing or SF signaling. An on-hook signal must be applied before redialing.	See A2S1	See A2S1, but numerals are not to be re-struck. Signal 'on-hook' before pressing REDIAL.

® Registered trademark

Table 3—4. Model TTS 59C Front Panel Indicators.

REF DES	NOMENCLATURE	DESCRIPTION
DS1	POWER	When lighted, indicates that POWER switch is ON and power is applied to unit.
DS2	T-R REV (WINK)	Indicates tip/ring polarity status on loop circuits. Normally lighted when tip more negative than ring. But, internal programming can reverse this indication.
DS3	E&M TWD. L	Indicates idle/busy status of E lead on line side of E&M circuits. Normally lighted for open or battery condition on E lead to indicate idle circuit. But, internal programming can change this indication.
DS4	E&M TWD.D	Indicates idle/busy status of M lead on drop side of E&M circuits. Normally lighted for ground or open condition on M lead to indicate idle circuit. But, internal programming can change this indication.

SECTION 4

THEORY OF OPERATION

4.1 This section contains the general and functional block diagram descriptions and the detailed circuit descriptions of the Model TTS 59C.

4.2 GENERAL BLOCK DESCRIPTION.

4.3 Signal connections and switching are shown in a simplified, general manner on Figure 4—1. Although signals are actually switched by relays controlled from the front panel, circuits are shown as if only switches are used. An understanding of the test set can be gained more readily with this simple approach. An inset identifies the major circuit categories discussed in the following paragraphs.

4.4 The line/drop, send/receive VF switching circuit accepts two- or four-wire VF connections via J9 through J12. Routing of signals to and from these connections is controlled by DROP/THRU/LINE switch S3 as follows.

(1) In THRU: Receive circuits are switched to send circuits (J9 to J11 and J12 to J10) and signals on the LINE jacks are bridged by the monitor function, through R_A and R_B.

(2) In DROP: The LINE jacks (J11 and J12) are terminated, the DROP REC 4W jack (J9) is switched to the measurement circuit, the DROP SEND 4W jack (J10) is switched to the test signal switching function, and the DROP jacks (J9 and J10) are bridged by the monitor function, through R_A and R_B.

(3) In LINE: The DROP jacks (J9 and J10) are terminated, the LINE REC 4W jack (J12) is switched to the measurement circuit, and the LINE SEND jack (J11) is switched to the test signal switching function, and the LINE jacks (J11 and J12) are bridged by the monitor function, through R_A and R_B.

4.5 The test signal switching function selects either a headset transmitter, an external oscillator, an external TMS instrument, internal in-band tone signaling, or internal loop dial pulses for sending into the circuit under test via DROP/THRU/LINE switch S3. The headset transmitter is enabled in either TALK positions of the DIAL + TALK 2W/KEY PULSE/TALK 4W switch S8. The in-band tone signaling is enabled only in the KEY PULSE position. An external or TMS instrument can be connected through J2 or J7 to TMS/THRU/SEND OSC switch S2. A relay (shown at the left-hand side of the pads block) senses tip-ring reversal on loop circuits under test and controls the T-R REV (WINK) indicator. Internally generated pulses control the relay for pulsing into a loop circuit under test. The pad controls act as follows.

(1) OdB: All operations toward the drop except in-band supervision, used for two-wire talk toward the line, including loop supervision and dialing.

(2) 7dB: Used for two-wire transmission loss tests an in-band addressing tone signaling toward the line.

(3) 16dB: Used for four-wire talk toward the line.

(4) 23dB: Used for four-wire transmission loss tests and in-band addressing toward the line.

(5) X + 12dB: Used for in-band (SF) supervision. X = 0, 7, or 23 dB.

When an oscillator or TMS instrument is set to supply +7 dBm to the TTS 59C, the pads deliver the correct levels to the circuit under test. Note that incoming signals from a two-wire line circuit under test can be delivered to TMS jack J7 (for measurement) and also to the internal monitor function.

4.6 The monitor and measurement function accepts signals from the line or drop side of a circuit under test, as selected by the DROP/THRU/LINE switch S3. These signals are combined (mixed) by R_A and R_B then amplified and switched to a headset receiver when the DIAL + TALK 2W/KEY PULSE/TALK 4W switch S4 is at KEY PULSE. When this switch is at TALK 4W (and TMS/THRU/SEND OSC switch S2 is at THRU) the headset receiver is connected to the selected REC jack (J9 or J12) through the measurement function. The headset is connected to the test signal switching function when the DIAL + TALK 2W/KEY PULSE/TALK 4W switch S8 is at DIAL + TALK 2W to complete the two-wire line circuit. (A muting function disables the headset receiver during dial pulsing when the DIAL + TALK 2W/KEY PULSE/TALK 4W switch S8 is in either TALK position). The measurement function:

(1) switches the selected REC jack to the TMS REC 4W jack (TMS/THRU/SEND OSC switch S2 at TMS),

(2) terminates the selected REC jack (TMS/THRU/-SEND OSC switch S2 at THRU, and DIAL ± TALK/KEY PULSE/TALK 4W switch S8 at DIAL ± TALK 2W),

(3) connects a four-wire circuit under test to the monitor as described previously.

4.7 The internal generator delivers dial pulses to the internal two-wire loop function and to the internal E&M switching function. Tones (SF, MF, or TT) are supplied to the test signal switching function. The in-band signaling **mode** is determined by the six-button array. Address **content** is determined by the keypad.

4.8 The E&M switching function is shown at the lower right in Figure 4—1. If the E&M TWD.L switch S5 and TWD.D switch S4 are at THRU and the DIAL L/CENTER/DIAL D switch S6 is at the CENTER position, the line E&M leads are carried through to the drop E&M leads. The drop M and line E leads are always monitored. The monitoring indicates E&M status. Thresholds in the monitor permit detection of voltage faults on these lines. Signaling to the circuit under test is initiated by moving either the TWD.L switch S5 or TWD.D switch S4 out of the THRU position. A voltage representing the off-hook position. With the DIAL L/CENTER/DIAL D switch S6 at DIAL L (or at DIAL D going toward the drop), the off-hook voltage is replaced with dial pulse voltages. Voltages representing the on-hook conditions are switched forward with the TWD.L and TWD.D switches at ON HK. the on-hook and off-hook voltages can be programmed to meet the needs of various trunk circuit types such as Type I, II, and III.

4.9 FUNCTIONAL DESCRIPTION

4.10 This discussion refers to Figure 6—1. The keypad assembly (keypad, dial pulse generator, and tone generator) and the E&M circuits are shown on sheet 2. The relay board switching functions are shown on sheet 1. An inset on sheet 1 identifies the four switching functions of the diagram. Logic symbol letters A through M shown on sheet 1 apply to this text. these letters are not part of the actual reference designators. The discussion proceeds in the following order:

- dial pulse generation,
- SF supervision,
- SF addressing,
- MF AND TT addressing,
- E&M switching,
- line/drop, send/receive switching,
- test signal switching,
- measurement switching,
- monitor switching.

4.11 DIAL PULSE GENERATION.

4.12 The TTS 59C generates dial pulses with a 61 percent break at a rate of ten per second. The dial pulse generator requires an off-hook control condition, DIAL PULSE (DP pushbutton) controls and accepts numerals 0 through 9 from the keypad. The generator also recognizes a REDIAL request and outpulses the last-inserted address in response to this command. Relay board OR-gate A senses the removal of ground in the OFF HK position of ON HK 2W/OFF HK 2W switch S7 and of E&M TWD.D and TWD.L switches S4 and S5. The output of gate A is applied through OR-gate B to AND-gate C. The logical product of $\overline{\text{OFF HK}}$ and DP is applied to gates E and F and through gate D to binary-to-phone pulse converter U1 located on dial pulse generator board A1A2.

4.13 The binary-to-phone pulse converter is quiescent with $\overline{\text{CALL REQUEST}}$ ($\overline{\text{CRQ}}$) high. The $\overline{\text{OUTPULSING}}$ (OPL) output is low in this state, as is the DIAL ROTATING OUTPUT (DRO). With the test set in an on-hook condition, gate E is not enabled. This forces it's output high and muting relay K2 is in the deenergized dial home state. When the logical product DP•OFF HK is produced as described in paragraph 4.12, $\overline{\text{OPL}}$ switches high. Gates E and F remain enabled and the relays do not change state. No dial pulses can be produced until the keypad is used.

4.14 The keypad pushbuttons are wired to produce a unique row and column signal combination for each pushbutton. Eight wires convey four-row data and four-column data signals to keypad-to-binary converter U2 located on A1A2. As the name implies, this circuit converts row and column data to a binary format. Also, the circuit produces an output pulse (AVAILABLE) when a numeral pushbutton is sensed. Each AVAILABLE pulse triggers a 100-microsecond strobe generator. The first strobe to the converter after the DP•OFF HK condition is set, dumps the old contents of pulse converter U1 and enters the data accompanying the strobe. Memory in pulse converter U1 stores succeeding numerals up to 16 numerals. The DRO and $\overline{\text{OPL}}$ outputs of U1 become active approximately 800 milliseconds after the first strobe. The $\overline{\text{OPL}}$ function applies a pulse to gate F, which pulses K1 on and off. The contact of K1 can be traced through S6, S4, and S5 to E&M board sending relays K2 and K3. It also goes through to S7 to loop off-hook relay K3 located on the relay board. These circuits are discussed in more detail in paragraph 4.31. The DRO output of U1 overlaps each burst of dial pulses present at OPL. The DRO output enables gate E to close muting relay K2. The contacts of K2 can be traced to the monitor circuit as discussed in paragraphs 4.43 through 4.45.

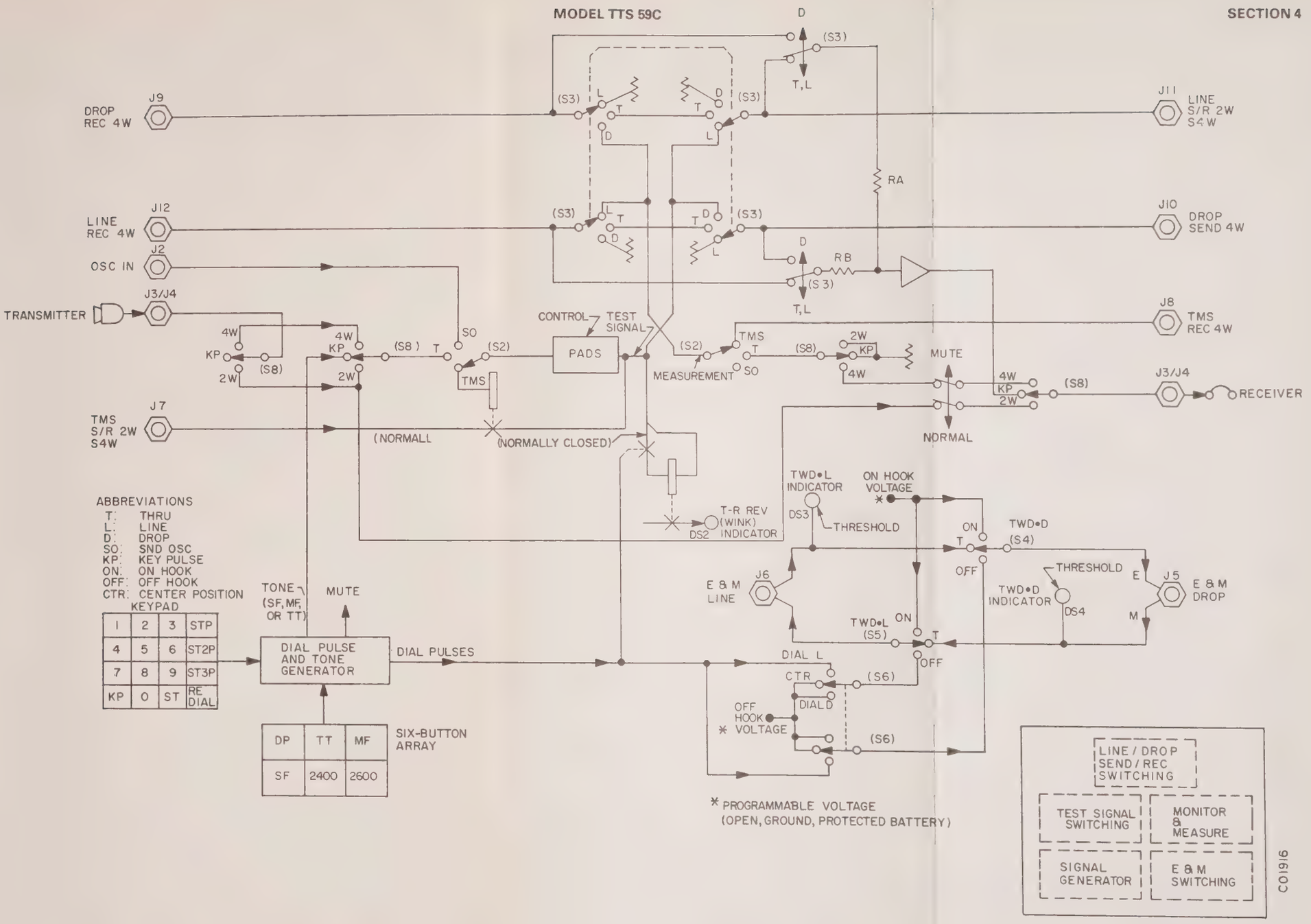


Figure 4—1. Model TTS 59C General Block Diagram.

4.15 The REDIAL signal causes the old contents in memory of pulse converter U1 to be outpulsed again but only after an on-hook signal is received from ON HK/OFF HK 2W switch S7, E&M TWD.D switch S4, or E&M TWD.L switch S5.

4.16 SF SUPERVISION.

4.17 The TTS 59C supplies a steady 2400- or 2600-Hz tone for signaling on-hook on an SF circuit. The generator requires that both the SF and either the 2400 or 2600 pushbuttons be latched. The generator on A1A3 is capable of producing all tones for SF, MF, and TT signaling. Read Only Memory (ROM) U3 contains data necessary for generating each in-band signaling frequency. Appropriate data is selected by control inputs supplied by the keypad binary data on A1A2, the mode on A2, and control circuit U1. The data supplied by ROM U3 and applied to programmable divider U4 controls the division of a 2 MHz clock. The division process produces frequencies that are 32 times the in-band signaling frequency. Binary counters U5 and U6 count the U4 outputs to produce binary outputs that cycle through 32 states for each cycle of the desired frequency. When sending SF, only counter U5 produces a cyclic output. The outputs of U5 and U6 address sine ROM U7. The contents of U7 represent sine wave amplitudes. Succeeding addresses produce a memory output that represents a sine wave function. Binary amplitude data is converted to an analog voltage by digital-to-analog converter U8. Amplifier U9 filters out the sine wave and then applies the signals to the circuit under test via transformer T1 and switching circuits located on relay board A3. Protection from transients is provided by CR2.

4.18 Latching of either the 2400 or 2600 pushbutton is sensed by gate H, located on A1A2. The resulting 100-microsecond strobe initiates the four-step control cycle of U1 located on A1A3. In conjunction with either the 2400 or 2600 input to control ROM U3, the control exerted by U1 on U3 serves to select two words in memory to be entered into divider U4. The set-up of the dial programmable divider requires both a control word and a data word for each frequency to be generated. The control exerted by U1 on divider U4 (ADDR and $\overline{\text{WRITE}}$) ensures that the memory outputs are accepted at the appropriate times during the control cycle. This control also ensures that the memory outputs are steered to the correct location on divider U4. The SF input to divider U4 inhibits counter 2 during SF operation.

4.19 Upon completion of the control cycle, control signals READY to sine ROM U7, located an A1A3. If gate I signals an active 2400 or 2600 output, and pulse converter U1 a low $\overline{\text{OPL}}$ signal, gate J generates a SEND signal. The active SEND signal, inverted by gate K, releases the reset from binary counter U5 and U6. The tone generator now sends the selected frequency to the circuit under test. Counter U6 produces no output at this time since counter 2 is inhibited.

4.20 Sending is continuous until an off-hook is to be signaled. Sending can be interrupted by releasing either the SF, 2400 or 2600 pushbutton. Normal procedures call for signaling off-hook by latching the DP pushbutton while leaving the SF pushbuttons latched. This sets $\overline{\text{OPL}}$ high via gates L and D and enables pulse converter U1 to receive an address.

4.21 SF ADDRESS SIGNALING

4.22 The TTS 59C sends SF addresses at the rate of 10 tone bursts per second at 61 percent break. Addressing requires that the SF and either the 2400 or 2600 pushbuttons be latched, that the DP pushbutton be latched, and that keypad numerals be pressed to designate the address. An on-hook is signaled (continuous SF tone) by releasing the DP pushbutton.

4.23 The tone generator operates as described in paragraphs 4.17 and 4.18. The conditioning of the SEND signal of A1A2 differs from that used during SF supervision. When the DP pushbutton is latched, gate L sets $\overline{\text{CRQ}}$ high through gate D. Converter U1 is now set to receive either an address or a REDIAL command. The $\overline{\text{OPL}}$ output goes high, disrupting the SEND signal, and the circuit remains quiet until the keypad is used. The first strobe produced when pressing numerals dumps the old contents of pulse converter U1 and enters the first new numeral. Pulse converter U1 proceeds to outpulse. Each pulse enables gate J to permit sending. The circuit again becomes quiet when addressing is completed. Note that the 100-microsecond strobe is inhibited by Gate H when using the keypad. Gate M cannot trigger the strobe generator while the non-inverting input to the trigger OR gate is held high.

4.24 MF AND TT SIGNALING

4.25 The TTS 59C sends standard two-of-six MF tones and standard TT pairs. MF and TT signaling requires that either the MF or TT pushbutton be latched and that the keypad be used.

4.26 The operation of the tone generator is similar to that described in paragraphs 4.17 and 4.18. Programmable divider U4 produces two outputs in the absence of the SF control input. The address to control ROM A1A3U3 now includes binary data from binary converter A1A2U2. The binary data alone accesses MF data while binary data accompanied by the TT control input accesses TT data. The four-step control cycle of A1A3U1 is initiated each time a pushbutton is pressed.

test and SF supervision levels. The test signal switching circuit also detects loop T-R reversal or wink inputs.

4.39 Test signal switching circuit switching is organized as follows.

- TMS (S2): TMS S/R S4W is switched to the pad circuit via J/JJ (TMS, K11).
- THRU (S2): Enables S8 functions (transmitter and in-band signaling).
- SEND OSC (S2): OSC IN is switched to the pad circuit via I/II (SEND OSC K12) and J/JJ (TMS, K11).
- DIAL + TALK 2W (S8): Connects transmitter to pad circuit via F/FF (TALK 2W, K14). Also, incoming voice is passed through this path, in reverse, to the monitor circuit (including contacts F/FF).
- KEY PULSE (S8): Connects in-band signaling to the pad via G/GG (TALK 2W, K14), H/HH (TALK 4W, K13), I/II (SEND OSC, K12), and J/JJ (TMS, K11).
- TALK 4W (S8): Connects transmitter to the pad via H/HH (TALK 4W, K13), I/II (SEND OSC, K12), and J/JJ (TMS, K11).

4.40 Pad control is described in paragraph 4.5. Tip-ring reversal circuit K1 and K2 is effective only when testing loop circuits. As described in paragraph 4.5, attenuation is 0 dB when operating toward the drop except during SF supervision and during line signaling and talking. Two-wire DP signaling must be accomplished with S8 set at DIAL + TALK 2W. In this condition, K15 interrupts the coil circuit of LINE•TALK relay K6 to prevent insertion of the 7 dB line circuit pad.

4.41 MEASUREMENT SWITCHING.

4.42 The TTS 59C switches VF inputs from circuits under test to the TMS REC 4W jack and switches unbridged four-wire VF signals to the monitor circuit as follows:

- TMS (S2): Contacts A/AA (DROP 2, K9) or A'AA' (LINE 1, K8) are switched to TMS REC 4W jack J8 via B/BB.
- THRU (S2): Enables S8 functions.
- SEND OSC (S2): Leaves selected circuit under test input (four-wire line or drop circuit) open.
- DIAL + TALK 2W or KEY PULSE (S8): terminates four-wire line (A'/AA') or drop (A/AA) input.
- TALK 4W (S8): Connects four-wire drop (A/AA) or line (A'/AA') circuit to monitor unbridged.

4.43 MONITOR SWITCHING.

4.44 The TTS 59C can switch bridged VF signals from circuits under test and test signals to the receiver. As explained in paragraph 4.42, unbridged four-wire VF inputs are switched by the measurement circuit to the monitor circuit by the test signal circuit as described in paragraph 4.38.

4.45 Switching is organized as follows.

- DIAL + TALK 2W: Incoming voice from line two-wire circuits under test is accepted from test signal switching circuit contacts F/FF (TALK 2W, K14) and switched through E/EE (KEY PULSE, K15) to the receiver.
- KEY PULSE: Bridged VF signals are accepted from line/drop, send/receive circuit contacts M/MM (DROP 3, K16) and P/PP (DROP 3, K16) amplified by U1C and U1D (channels A and B respecitively), mixed by R24 and R26, amplified by U1A and Q1, and switched by E/EE (KEY PULSE, K15) to the receiver.
- TALK 4W: Unbridged four-wire inputs are accepted from measurement circuit contacts D/DD (TALK 4W, K13) and switched through E/EE (KEY PULSE, K15) to the receiver.
- Pins 10 and 11 of A3J1 are shorted by muting relay A1A2K2 via pins 21 and 22 of A3J3 and E/EE (KEY PULSE, K15) during outpulsing.

4.46 DETAILED CIRCUIT DESCRIPTIONS.

4.47 Detailed circuit descriptions are provided for circuits not fully explained by the functional descriptions. Subjects are discussed in the following order.

- Power distribution
- Dial pulse generator
- Clocks
- Tone generator control
- Tone Generator sine ROM
- E&M send circuit
- E&M receive circuit

4.49 Distribution of input and derived power is illustrated on Figure 4—2. The input power supplied by the CO battery or an accessory supply via J1 is applied through F1 and S1 to A2J3 and A3J4. Reference diode DR7 sets the emitter of Q7 at approximately —22 V. Regulators U4 and U5 supply —15 V and —5 V to circuits A1A1, A1A2, A1A3, A2, and A3. Reference diode CR2 on A1A3 supplies —6.2 V to the tone generator analog circuits.

4.50 DIAL PULSE GENERATOR.

4.51 The keypad and dial pulse generator schematics are shown on Figure 6—5. Dial pulse generator timing is shown on Figure 4—3. This discussion relates the control and keypad inputs applied to A1A2 to the production of the muting and dial pulse outputs. With $\overline{\text{ON HK}}$ low at J2-26, $\overline{\text{CRQ}}$ at U6-13 is high. When $\overline{\text{CRQ}}$ is high, $\overline{\text{OPL}}$ and DRO at U1-11 and U1-12 are low. Under these conditions, U3-3 and U3-5 are low, dial pulses relay K1 is energized, and muting relay K2 is de-energized.

4.52 When $\overline{\text{ON HK}}$ goes high, $\overline{\text{CRQ}}$ goes low. The DRO output of U11 remains low but the $\overline{\text{OPL}}$ output goes high. Pulse converter U1 is now internally prepared to receive a REDIAL or STROBE input. The outputs at U3-3 and U3-5 remain low and relays K1 and K2 do not change state.

4.53 Keypad-to-binary converter U2 receives row and column inputs from the keypad. When a pushbutton is pressed, DATA AVAILABLE appears at U2-12 to produce STROBE AT U4-6 and U1-3. The first STROBE applied to U1 dumps the old contents of the internal memory of U1 and enters the new binary-coded-keypad data. Approximately 800 milliseconds after the first strobe, $\overline{\text{OPL}}$ starts pulsing. Also, the DRO output switches high approximately 100 milliseconds before the first pulse appears at $\overline{\text{OPL}}$. Dial pulse relay K1 opens when $\overline{\text{OPL}}$ is low. Muting relay K2 closes when DRO is high. The DRO output remains high for approximately 100 milliseconds after the end of the last pulse from $\overline{\text{OPL}}$. The memory contents of U1 are pulsed out in a sequence of first in, first out when REDIAL is requested. The memory can hold up to 16 digits.

4.54 CLOCKS.

4.55 A 40-kHz rectangular wave is produced on A1A2 by U5B, R2, and C7, which make up a CMOS oscillator. Capacitor C7 alternately charges to the logic high threshold and discharges to the logic low threshold. The 40-kHz wave clocks the tone generator control circuits.

4.56 A 2-MHz clock is produced by U7 and Y1 located on A1A2. The internal circuit of U7 is designed to minimize coupling to the supply voltage source by using a separate bus to the oscillator circuit.

4.57 TONE GENERATOR CONTROL.

4.58 The tone generator schematic diagram is shown on Figure 6—7. The control circuit includes U1 and associated logic elements U10B, U2A, U2C, and U2F. The control timing is shown on Figure 4—4. For each SF, MF, or TT request, the control circuit must coordinate the transfer of data from control ROM U3 to dual programmable divider U4. The dividers then produce clocks at rates that are 32 times the requested signaling frequency. This discussion relates the 50-kHz clock, the STROBE, and ROM U3 addressing signals to the set up of the dividers in U4. When this circuit is not processing a request, U1-3 is low and U1B holds a count of 4. Thus READY is high. The READY signal at U1-1 disables the 50kHz clock and U1A does not count. The A_0 and A_1 inputs to ROM U3 are low and the A_0 and A_1 inputs to divider U4 are high.

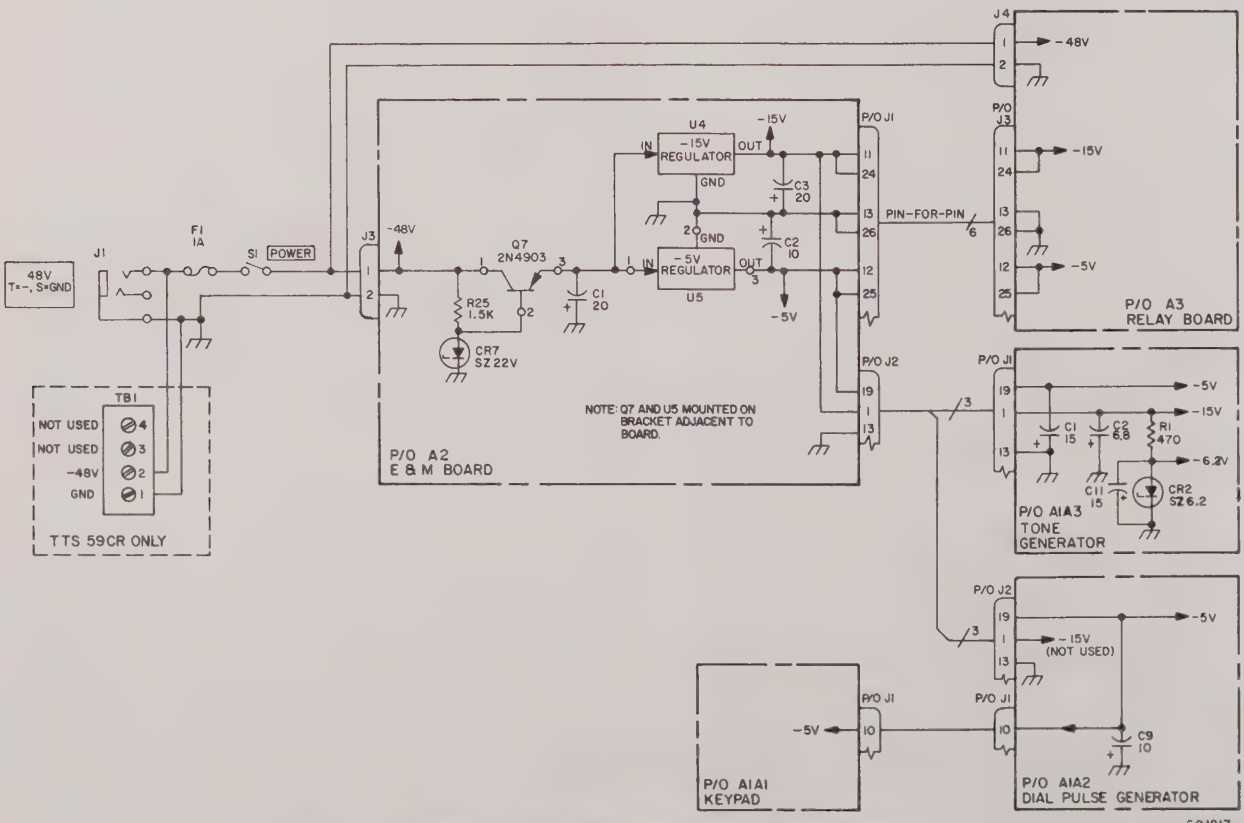


Figure 4—2. Model TTS 59C Power Distribution Diagram.

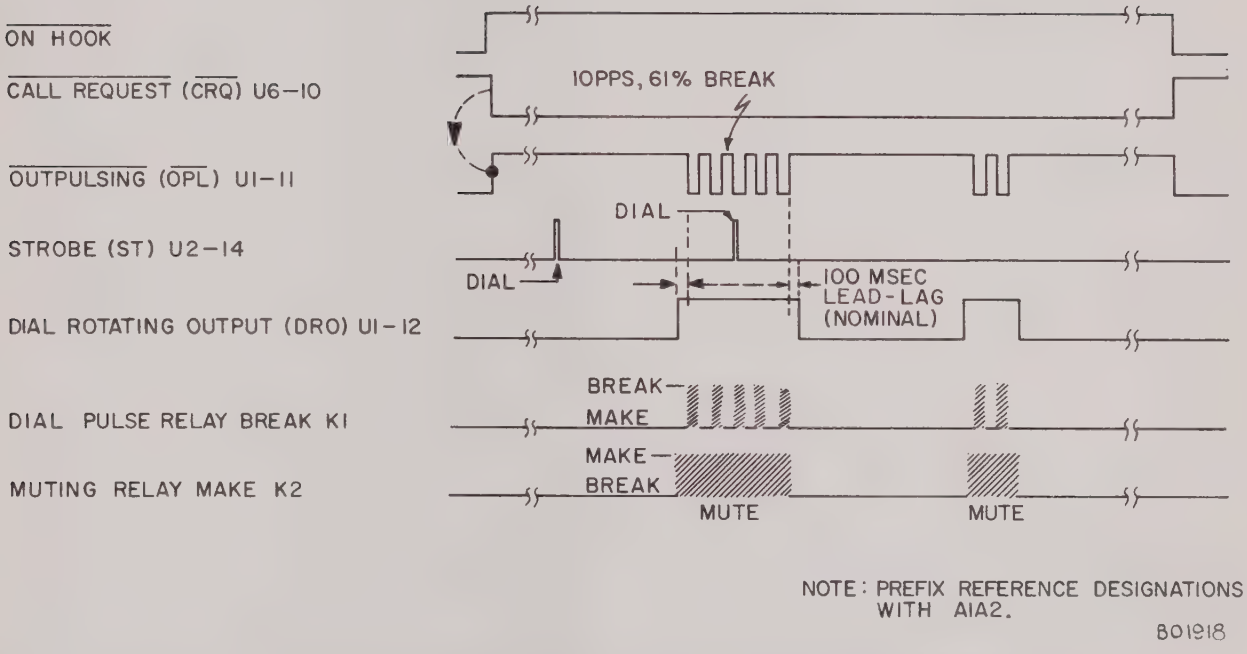


Figure 4—3. Dial Pulse Timing For Loop and E&M Addressing.

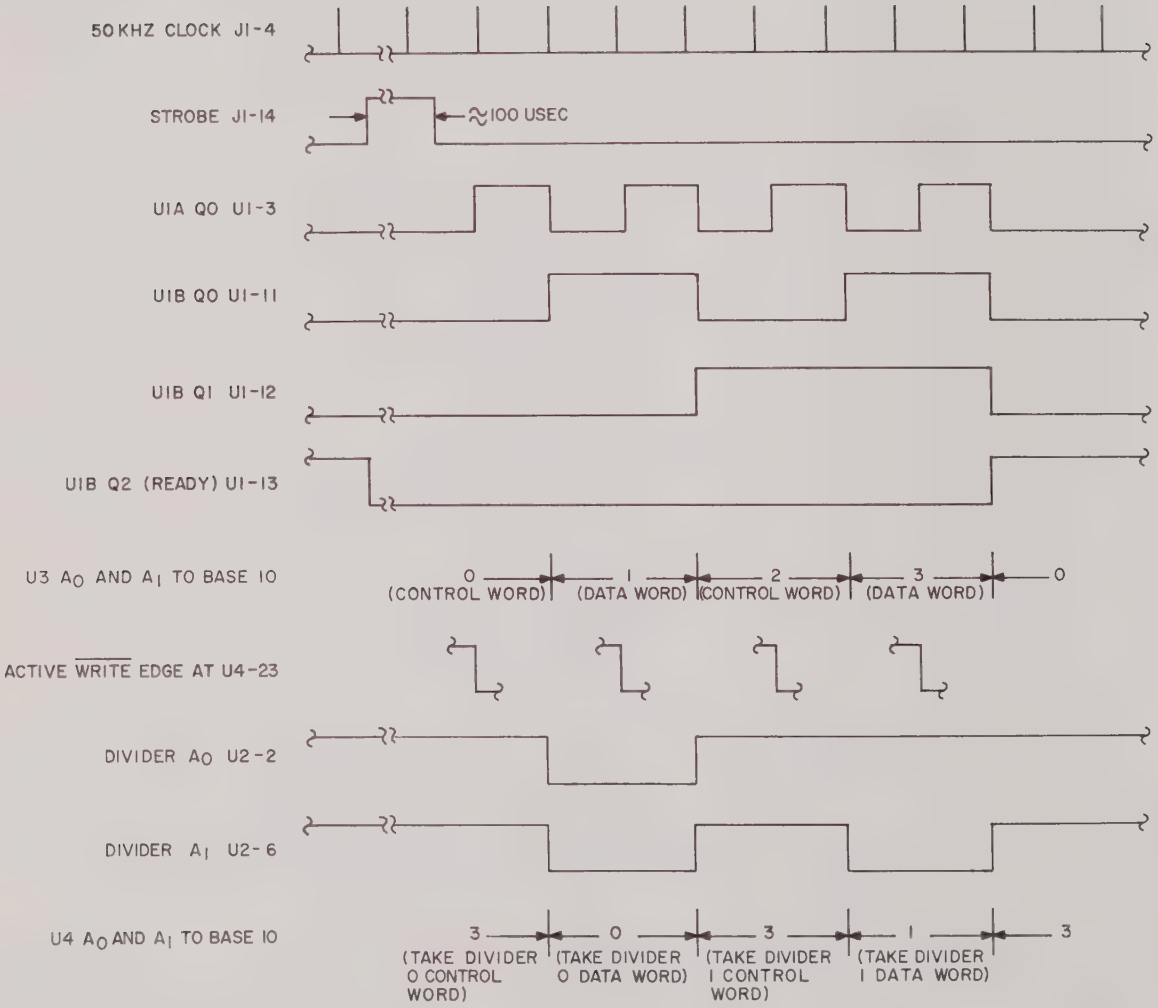


Figure 4—4. Tone Generator Control Timing.

4.59 The STROBE appears when a keypad pushbutton is pressed (unless either the 2400 or 2600 pushbutton is latched) or upon closure of the contacts of either the 2400 or 2600 pushbutton. The STROBE is accompanied by appropriate A_2-A_8 inputs to control ROM U3. The combination of these inputs, along with those at A_0 and A_1 supplied by U1B, make up the control ROM address. Data stored in each legitimate ROM address controls the production of each in-band signaling frequency or combination of frequencies. The STROBE resets U1A and U1B. The READY signal goes low and the control levels at the A_0 and A_1 inputs to U3 and U4 remain unchanged (i.e., at the address of divider 0 control word). The 50-kHz clock is now free to trigger U1A. Refer now to Figure 4—4 to trace the sequence outlined as follows.

1st positive edge at U1-3: write divider 0 control word (U4).
1st negative edge at U1-3: set address of divider 0 at data word (U3).
2nd positive edge at U1-3: write divider 0 data word (U4).
2nd negative edge at U1-3: set address of divider 1 control word (U3).
3rd positive edge at U1-3: write divider 1 control word (U4).
3rd negative edge at U1-3: set address of divider 1 data word (U3).
4th positive edge at U1-3: write divider 1 data word (U4).
4th negative edge at U1-3: send READY to U7.

4.60 Each programmable divider generates a frequency that is 32 times the requested signaling frequency. For example, if the digit 4 is to be sent as an MF addressing digit, the divider would produce 22,400 and 41,600 clock pulses per second to yield 700- and 1300-Hz tones. The 2 MHz divider input clock would have to be divided by 89.3 and 48.1 respectively to produce these clock rates. Division is by whole integers only, however. Choosing the nearest integer, division by 89 and 48 will produce 22,472 and 41,667 pps clocks. When divided by 32, these yield 702 and 1302 Hz tones. The two divisors of 89 and 48 are among the data transferred from U3 to U4 during the control sequence described above to send the digit 4 in the MF sending mode. One divider is disabled in the SF mode.

4.61 TONE GENERATOR SINE ROM.

4.62 Ripple counters U5 and U6 supply five-level outputs to sine ROM U7. Because the input clock to the ripple counter is at a rate of 32 times the desired frequency, 32 counts (counts 0 through 31) will be sent to the sine ROM for each cycle of the desired output frequency. The organization of data in U7 can be best understood by first considering the events that occur in the SF mode when only U5 is enabled. In this mode, only addresses 0 through 31 of U7 are called up. Each address contains data representing a voltage at a particular point on a sine wave is built up incrementally. A plot as shown on Figure 4—5 is obtained when the addresses are read out in order. Addresses 0 through 31 are shown across the bottom. Projecting upwards, an output magnitude is found in parenthesis for each address. These are connected by solid lines to show an incremental sive wave that would be produced by D-to-A converter U8.

4.63 E&M SEND CIRCUIT.

4.64 The TTS 59C can send open ground, or protected battery to represent on-hook or off-hook conditions. Selection is independent for the line M lead and the drop E lead. The E&M circuit board is shown on Figure 6—9. Sections 7 through 10 of switch S7 send toward the line while sections 7 through 10 of switch S8 send toward the drop. Sections 7 and 8 of each switch select the on-hook condition and sections 9 and 10 select the off-hook condition refer to Table 4—1 for send supervision selection.

Table 4—1. E&M Supervision Selections

SUPERVISION CONDITION APPLIED AT LINE M LEAD J1—7 (DROP E LEAD J1—10)	SWITCH S7 (S8) SECTION				RELAY K3 (K2)
	7	8	9	10	
On-hook . . . open	OFF	OFF			de-energized
On-hook . . . battery	ON	OFF			de-energized
On-hook . . . ground	OFF	ON			de-energized
Off-hook . . . open			OFF	OFF	energized
Off-hook . . . battery			ON	OFF	energized
Off-hook . . . ground			OFF	ON	energized

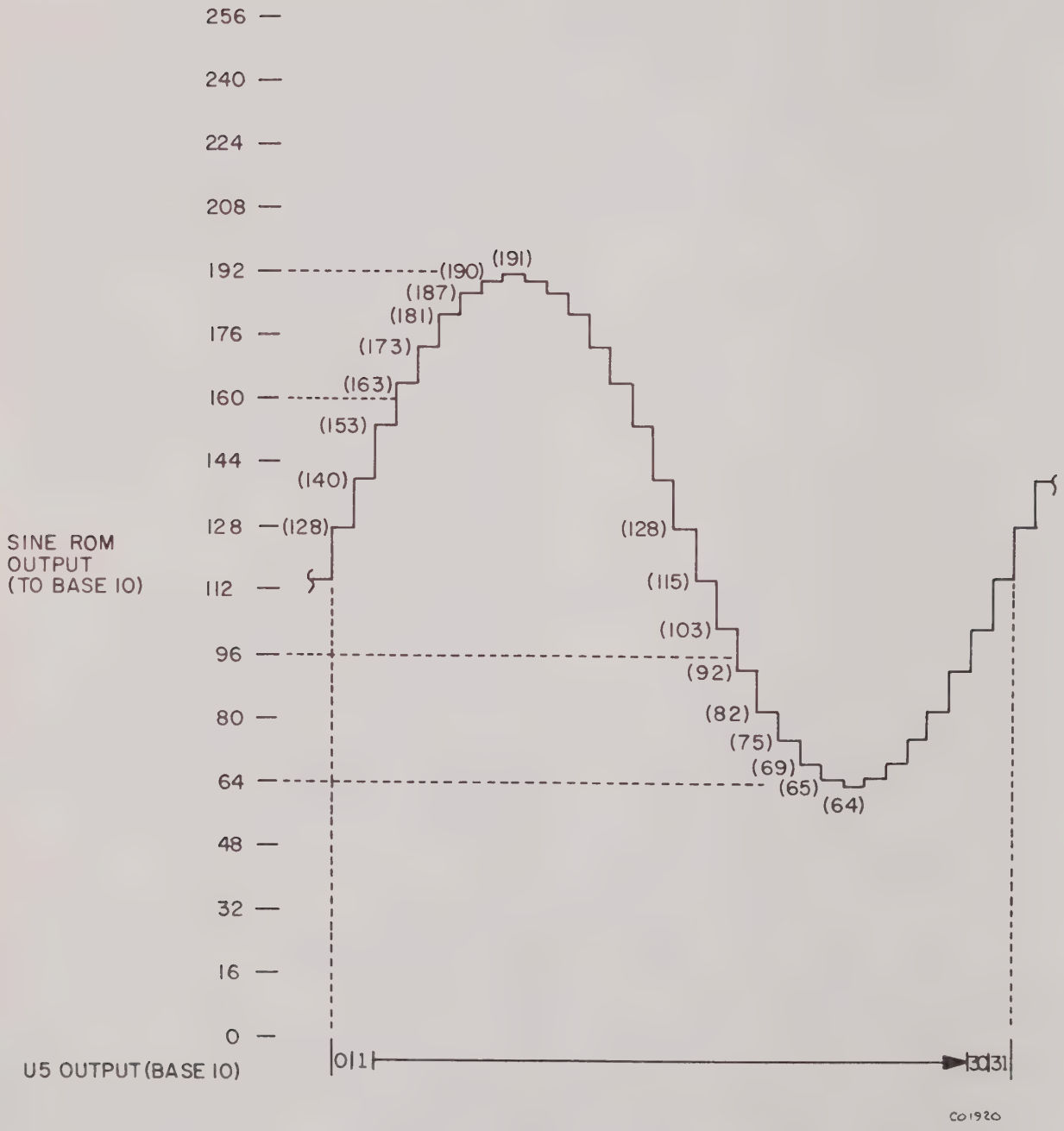


Figure 4—5. Sine ROM Output For A Single Input.

4.65 E&M RECEIVE CIRCUIT.

4.66 The monitor circuit threshold can be set independently by sections 1 through 4 of switch S7 (drop M lead) and switch S8 (line E lead). Each section selects a different value of resistance in a voltage divider network. The voltage at the junction of the divider is the reference for the associated comparator. A comparator output will be high when the input at pin 2 is more positive than the reference and low when this input is more negative. The monitored lead is connected through a diode to a voltage divider . . . R18/R19 in the drop M lead circuit and R5/R4 in the line E lead circuit.

4.67 Input voltages required to trip the comparator circuits are listed in Tables 4—2 and 4—3. If the drop M lead circuit is receiving an open or an input more positive than one diode drop (μ 0.5 V) the voltage at pin 2 of the comparator will be 0Vdc. Similarily if the line E lead circuit sees an input one diode drop more negative than —15 V, the voltage at pin 2 of its comparator will be —15 V. The approximate voltage at the comparator for the drop M lead circuit is (X + 0.5) ÷ 2.02, where X is more negative than —0.5V. Likewise, the voltage at the comparator for the line E lead circuit is (Y—0.5) ÷ 1.05, where Y more positive than —14.5V.

Table 4—2 Monitor Thresholds

SWITCH S7 SECTION	REFERENCE VOLTAGE	INPUT THRESHOLD
1	—1.4V	—3.3V
2	—2.3V	—5.2V
3	—5.0V	—10.6V
4	—6.0V	—12.6V

Table 4—3 E-Lead Monitor Thresholds

SWITCH S8 SECTION	REFERENCE VOLTAGE	INPUT THRESHOLD
1	—3.9V	—2.8V
2	—5.8V	—4.8V
3	—11.1V	—10.4V
4	—13.4V	—12.8V

4.68 Switch sections 5 and 6 of S7 (drop) or S8 (line) set the manner in which the E&M TWD.L and TWD.D indicators operate. The normal manner is considered to be that case where the indicator is lighted when the circuit under test is idle. the indicators are returned to ground. Thus, an indicator will be lighted when —4.5V is at the output of the detector. Tables 4—4 and 4—5 summarize the switch settings as set at the factory prior to shipment.

Table 4—4 M Lead Switch S7 Factory Settings

SWITCH S7 SECTION	SETTING	RESULT
1	OFF	Selects —12.6 as threshold
2	OFF	
3	OFF	
4	ON	
5	ON	TWD.D indicator on if idle . . .
6	OFF	ground or open on M lead
7	OFF	Sends ground on line M lead as
8	ON	on-hook
9	OFF	Send protected battery on line
10	ON	M lead as off-hook

Table 4—5 E Lead Switch S8 Factory Settings

SWITCH S8 SECTION	SETTING	RESULT
1	OFF	Selects —12.8 as threshold
2	OFF	
3	OFF	
4	ON	
5	ON	TWD.L indicator on if idle . . .
6	OFF	battery or open on E lead
7	OFF	Sends open on drop E lead as
8	ON	on-hook
9	OFF	Sends ground on drop E lead as
10	ON	off-hook

SECTION 5

MAINTENANCE AND CALIBRATION

5.1 No adjustment or calibration is required for the Model TTS 59C. No maintenance is prescribed.

SECTION 6

DIAGRAMS

6.1 This section contains the functional block diagrams, parts location diagrams, and schematic diagrams for the Model TTS 59C.

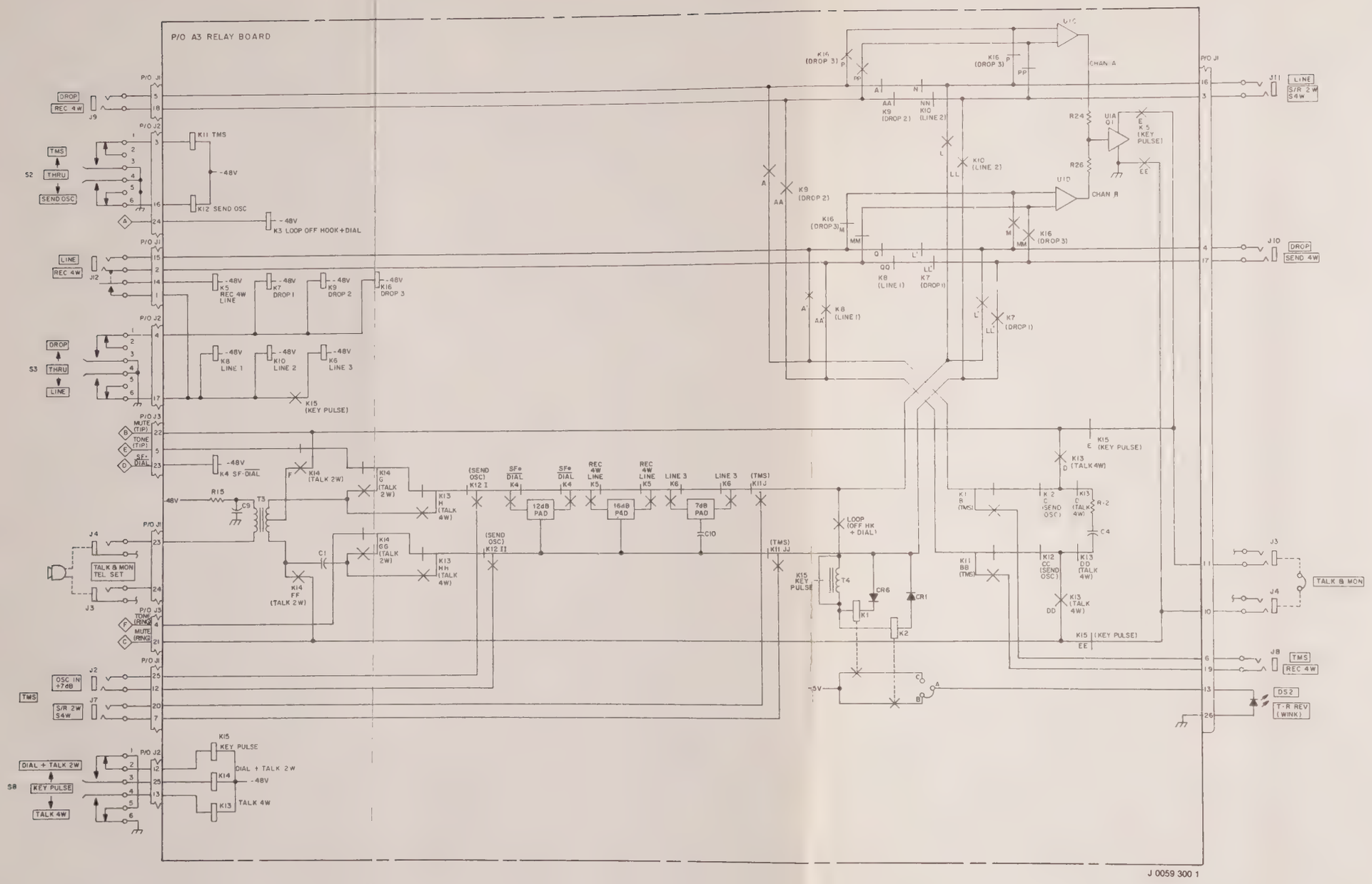


Figure 6—1. Model TTS 59C Functional Block Diagram. (Sheet 1 of 2)

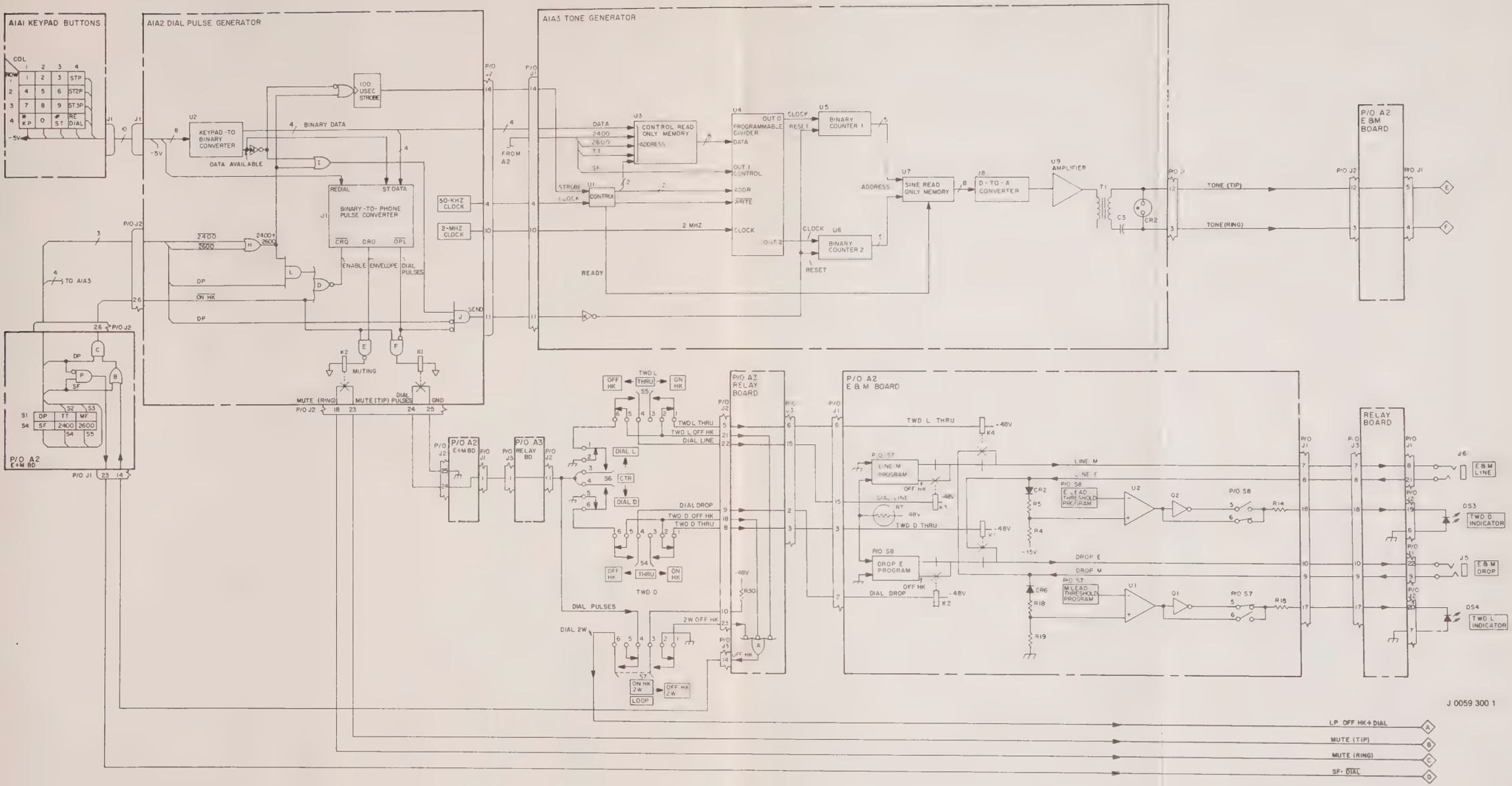


Figure 6—1. Model TTS 59C Functional Block Diagram. (Sheet 2 of 2)

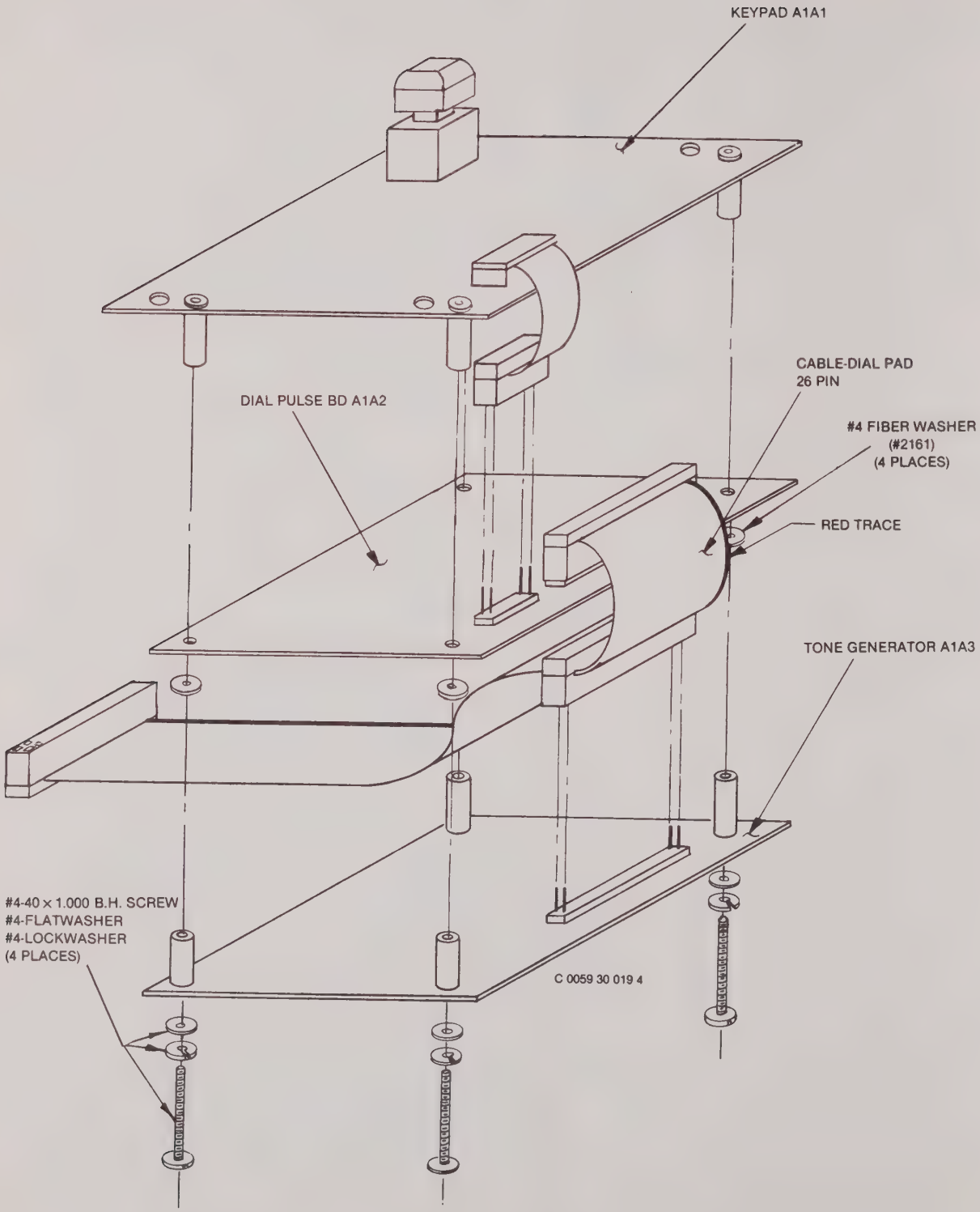
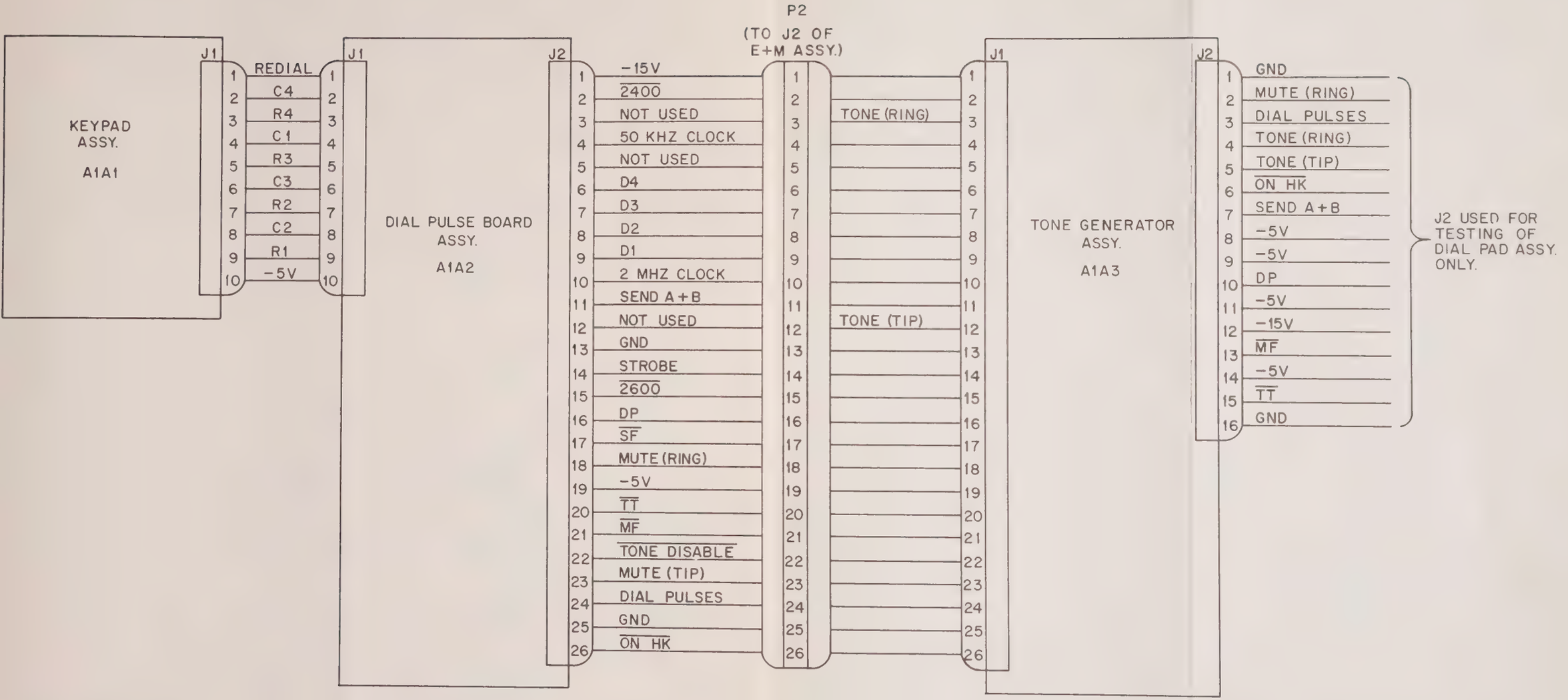


Figure 6—2. Dial Pad Assembly A1 Parts Location Diagram.



KEYPAD	
NE PART NO	B0059-30-018
REF DESIG	A1A1
PC NO	96910

DIAL PULSE	
NE PART NO	B4000-01-014
REF DESIG	A1A2
PC NO	96888

TONE GENERATOR	
NE PART NO	B0059-30-012
REF DESIG	A1A3
PC NO	96887

C 0059 30 019 1

Figure 6—3. Dial Pad Assembly A1 Schematic Diagram.

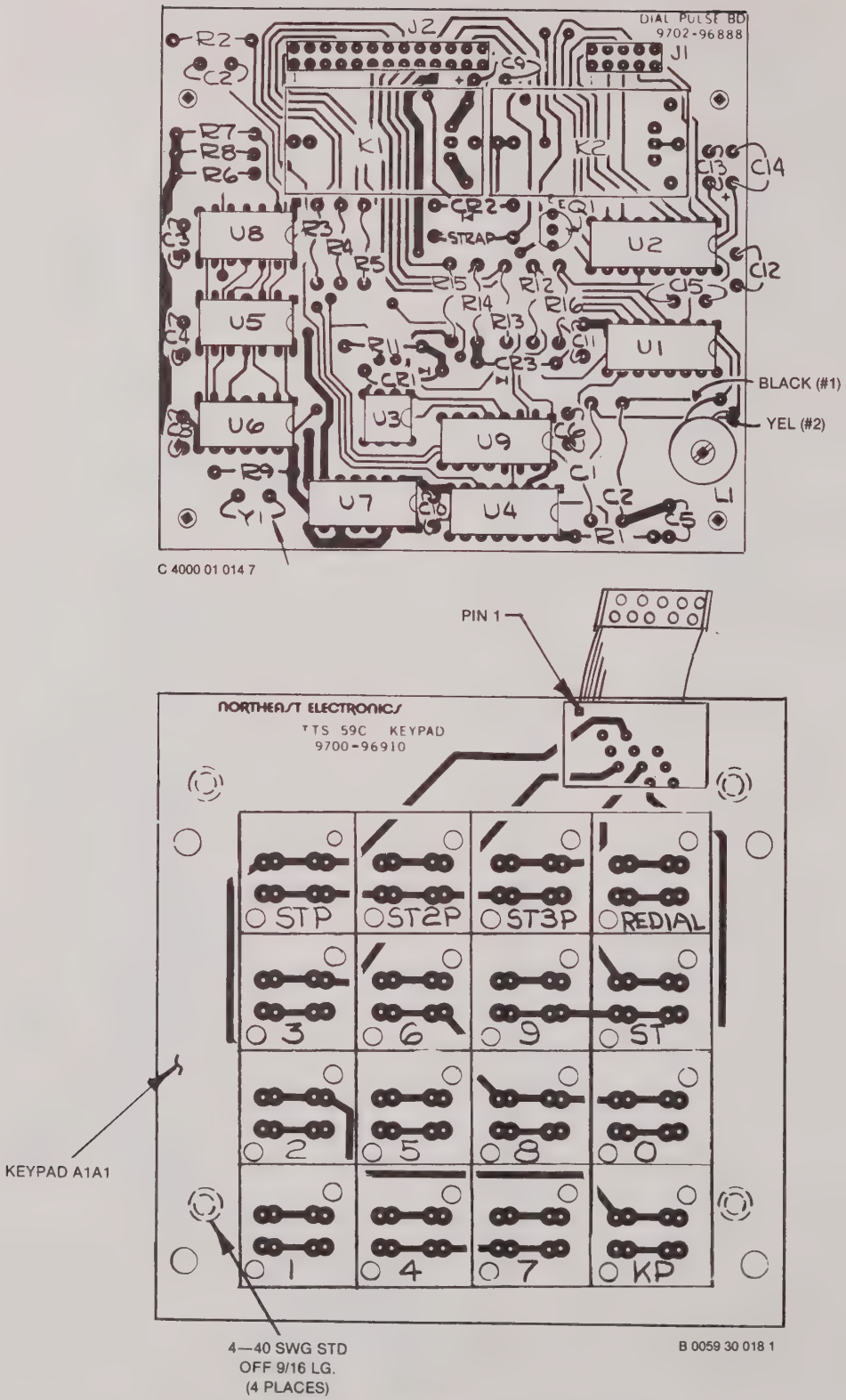
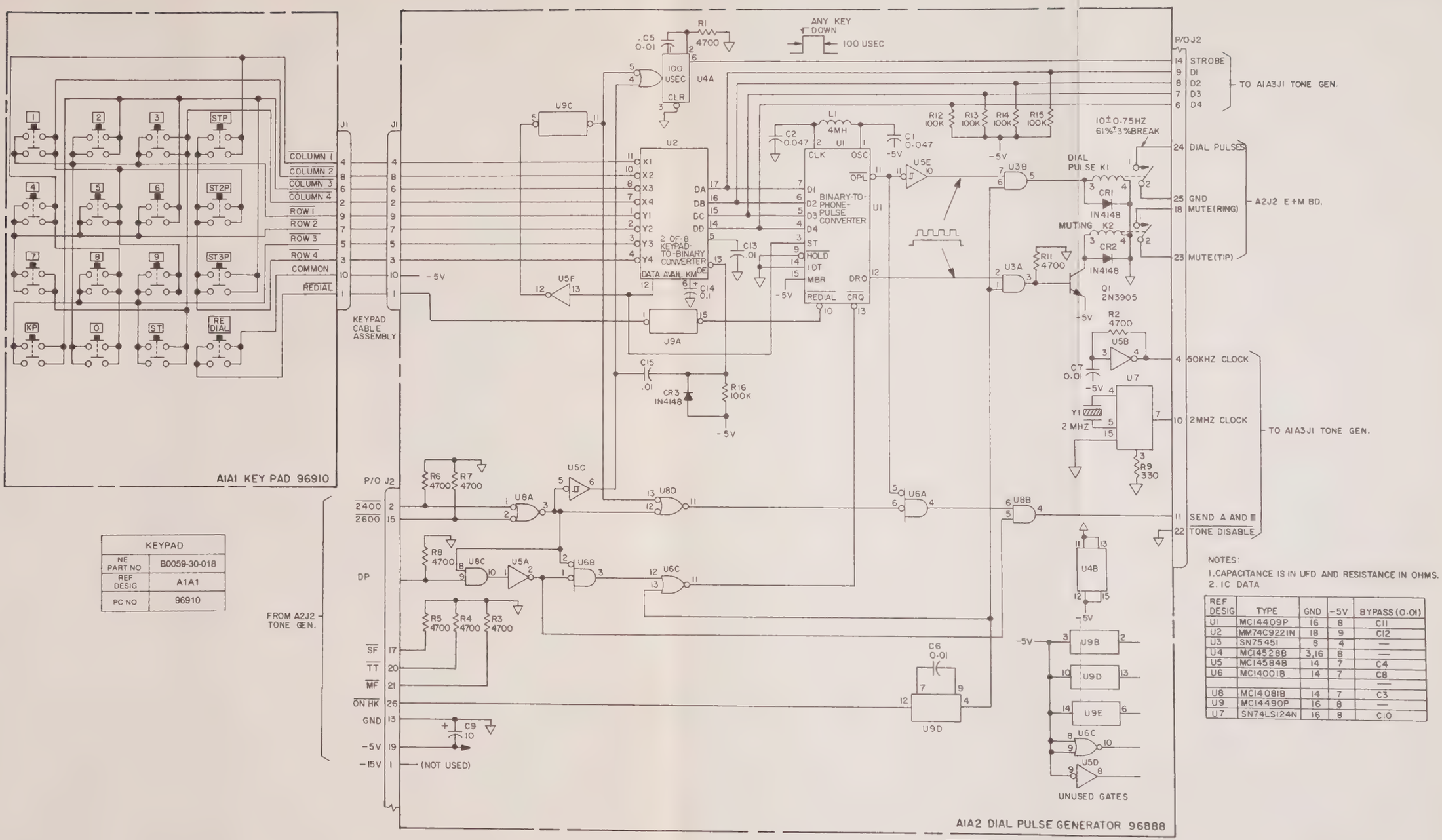


Figure 6—4. Keypad A1A1 and Dial Pulse Generator A1A2 Parts Location Diagram.



KEYPAD	
NE PART NO	B0059-30-018
REF DESIG	A1A1
PC NO	96910

DIAL PULSE	
NE PART NO	B4000-01-014
REF DESIG	A1A2
PC NO	96888

D 0059 30 318 1

NOTES:
1. CAPACITANCE IS IN UFD AND RESISTANCE IN OHMS.
2. IC DATA

REF DESIG	TYPE	GND	-5V	BYPASS (0.01)
U1	MC14409P	16	8	C11
U2	MM74C922IN	18	9	C12
U3	SN75451	8	4	—
U4	MC14528B	3,16	8	—
U5	MC14584B	14	7	C4
U6	MC14001B	14	7	C8
				—
U8	MC14081B	14	7	C3
U9	MC14490P	16	8	—
U7	SN74LS124N	16	8	C10

Figure 6–5. Keypad A1A1 and Dial Pulse Generator A1A2 Schematic Diagram.

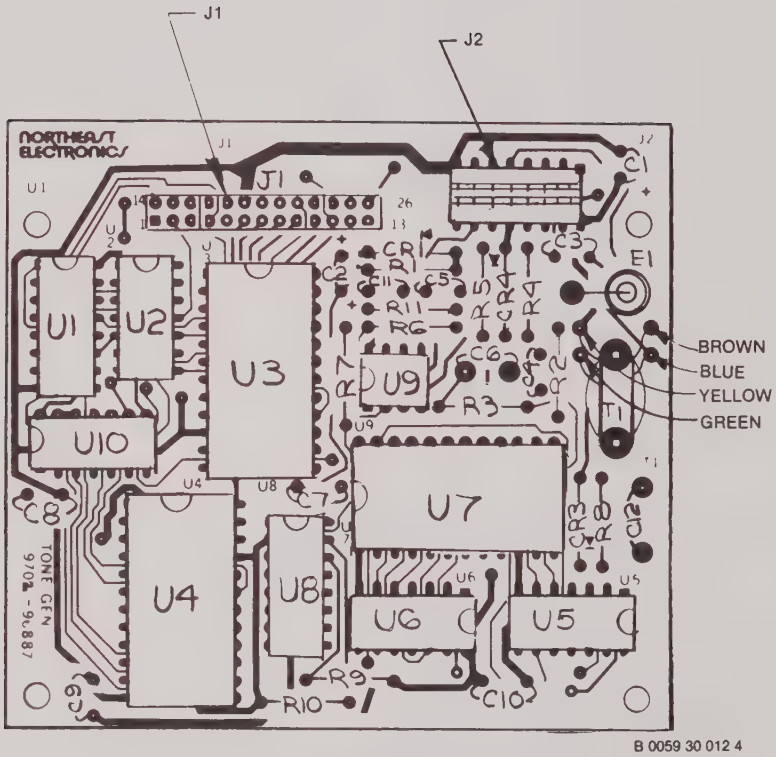
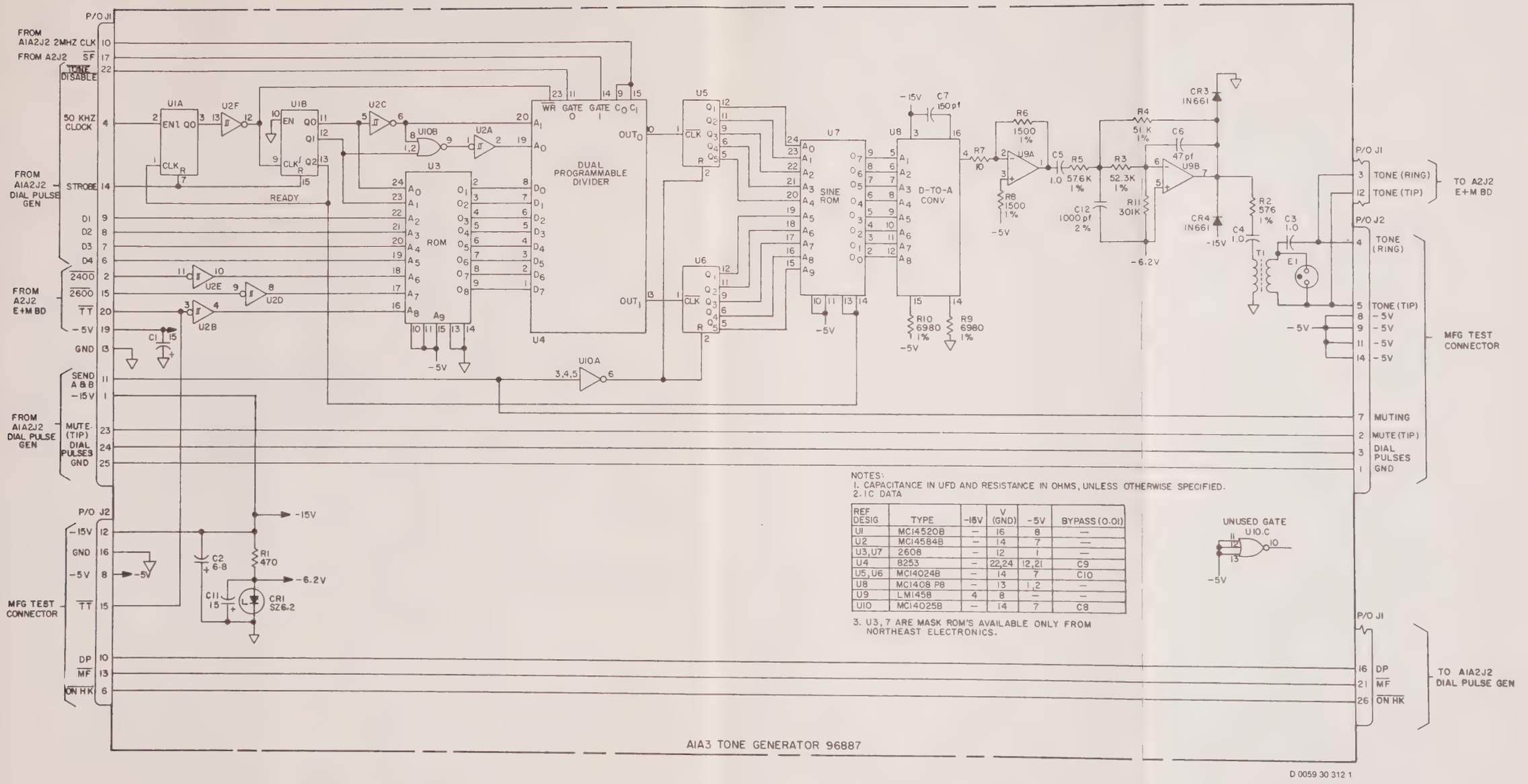


Figure 6—6. Tone Generator A1A3 Parts Location Diagram.



NOTES:
1. CAPACITANCE IN UFD AND RESISTANCE IN OHMS, UNLESS OTHERWISE SPECIFIED.
2. IC DATA

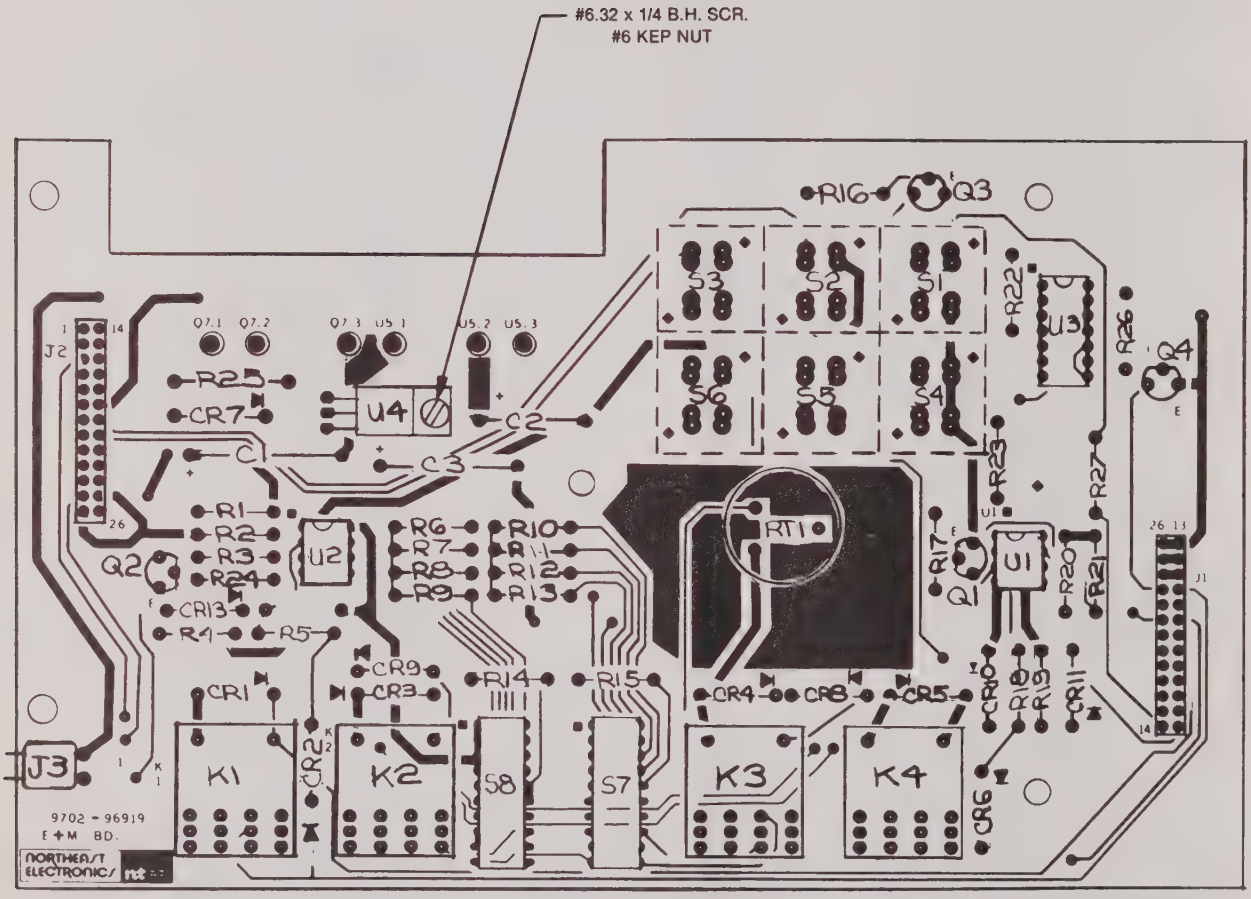
REF DESIG	TYPE	-15V	V (GND)	-5V	BYPASS (0.01)
U1	MC14520B	—	16	8	—
U2	MC14584B	—	14	7	—
U3,U7	2608	—	12	1	—
U4	8253	—	22,24	12,21	C9
U5,U6	MC14024B	—	14	7	C10
U8	MC1408 P8	—	13	1,2	—
U9	LM1458	4	8	—	—
U10	MC14025B	—	14	7	C8

3. U3, 7 ARE MASK ROM'S AVAILABLE ONLY FROM NORTHEAST ELECTRONICS.

D 0059 30 312 1

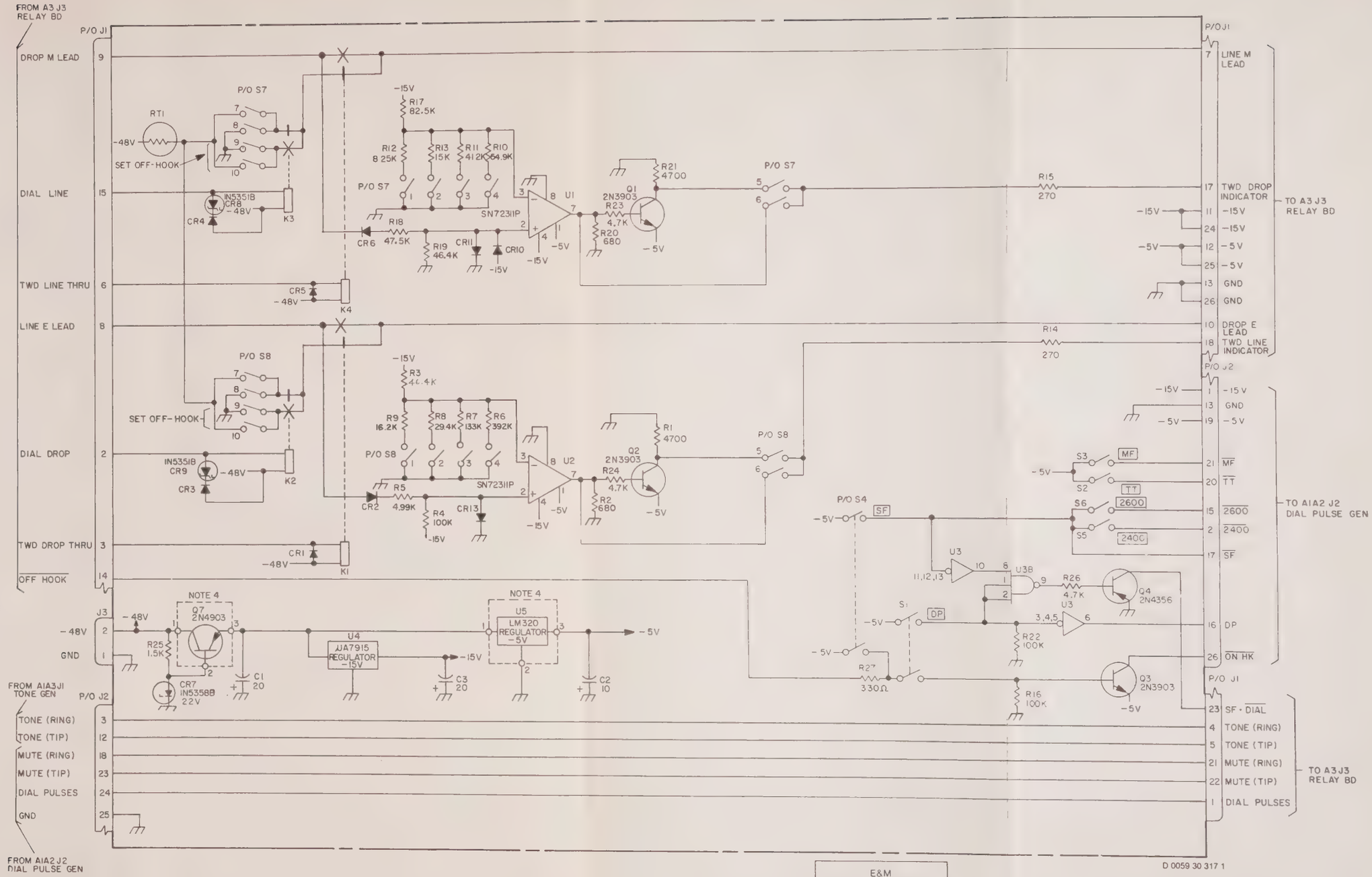
TONE GENERATOR	
NE PART NO	B0059-30-012
REF DESIG	A1A3
PC NO	96887

Figure 6—7. Tone Generator A1A3 Schematic Diagram.



C 0059 30 017 3

Figure 6—8. E&M Board A2 Parts Location Diagram



NOTES:
1. INTERCONNECTIONS
   J1: PIN-FOR-PIN TO A3J3
   J2: PIN-FOR-PIN TO A1A2J2, A1A3J1
2. ALL CAPACITANCE IN MICROFARADS AND RESISTANCE IN OHMS.
3. ALL DIODES IN4006 UNLESS OTHERWISE SPECIFIED.
4. MOUNTED ON BRACKET ADJACENT TO BOARD.

E&M	
NE PART NO	C0059-30-017
REF DESIG	A2
PC NO	96919

Figure 6—9. E&M Board A2 Schematic Diagram.

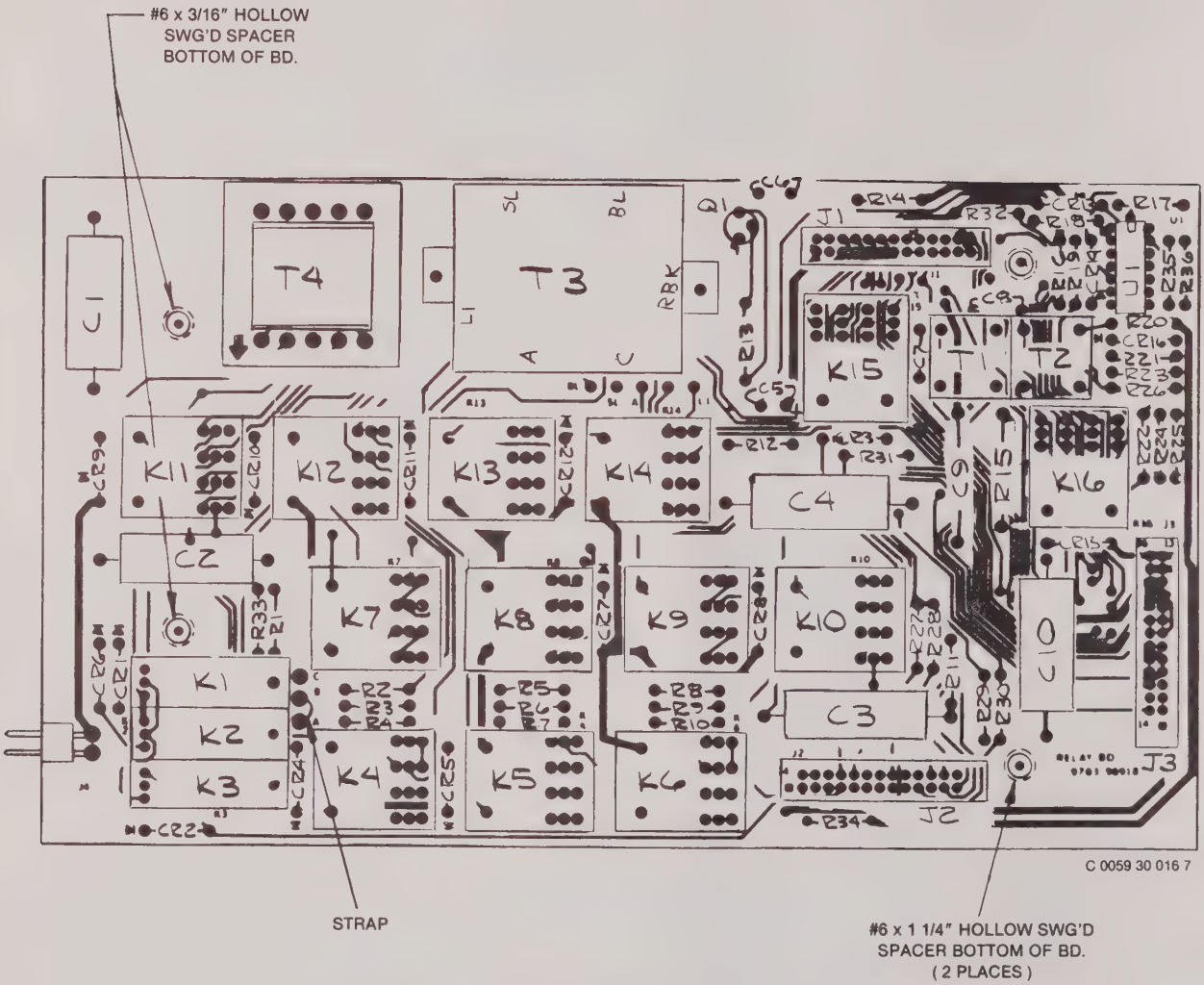
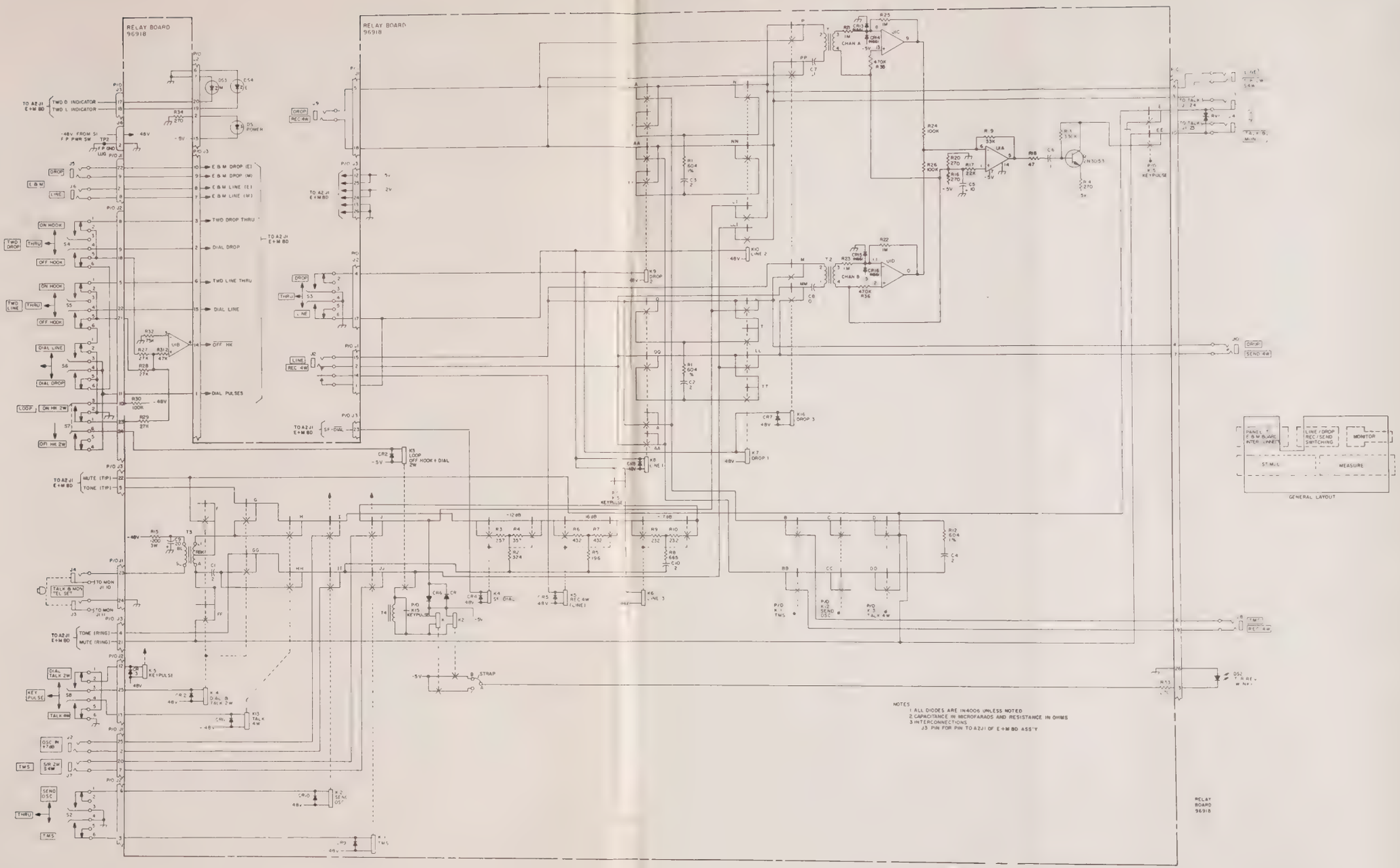


Figure 6—10. Relay Board A3 Parts Location Diagram.



D 0059 30 316 3

RELAY	
NE PART NO	C0059-30-016
REF DESIG	A3
PC NO	96918

Figure 6—11. Relay Board A3 Schematic Diagram.

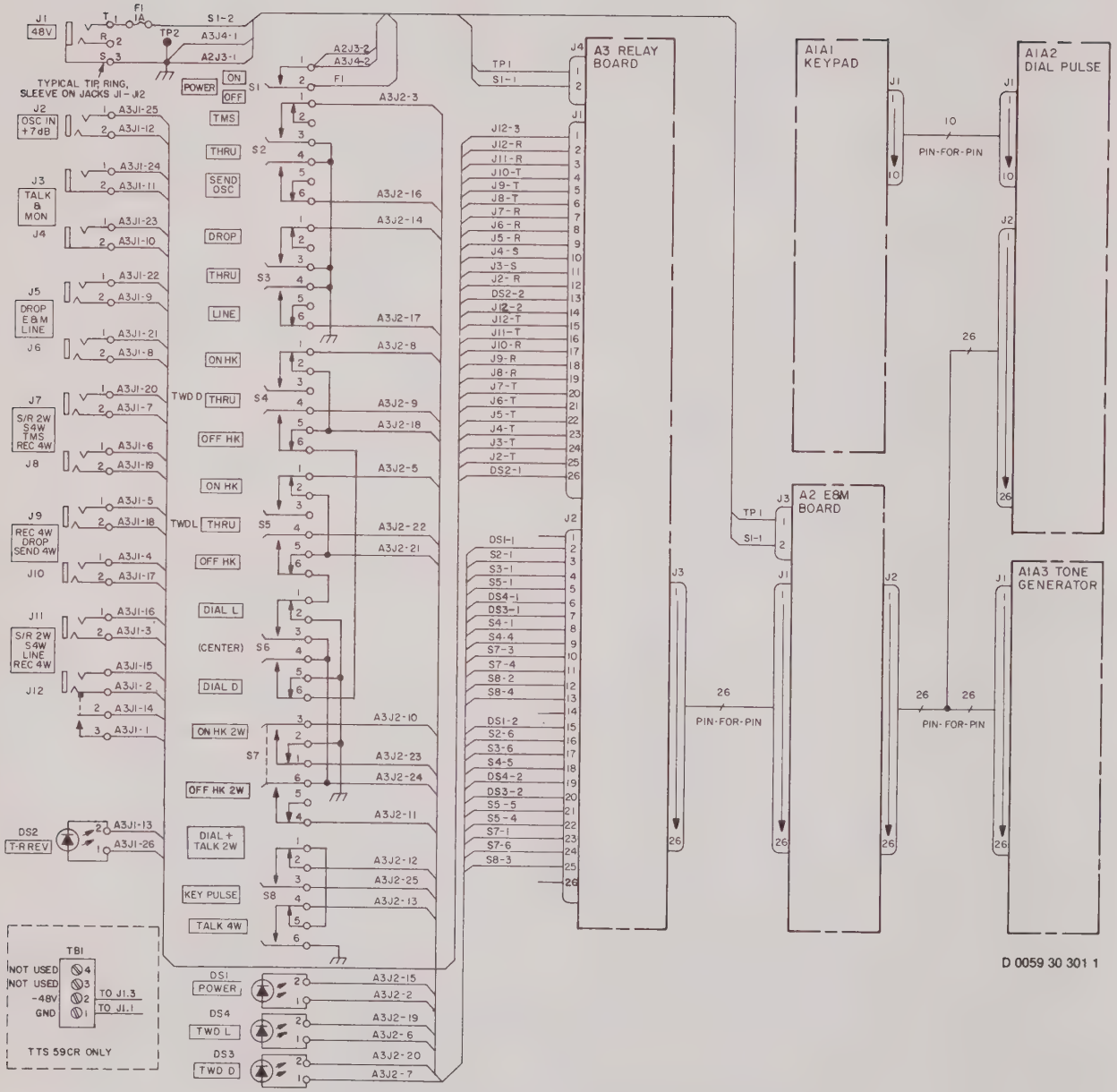
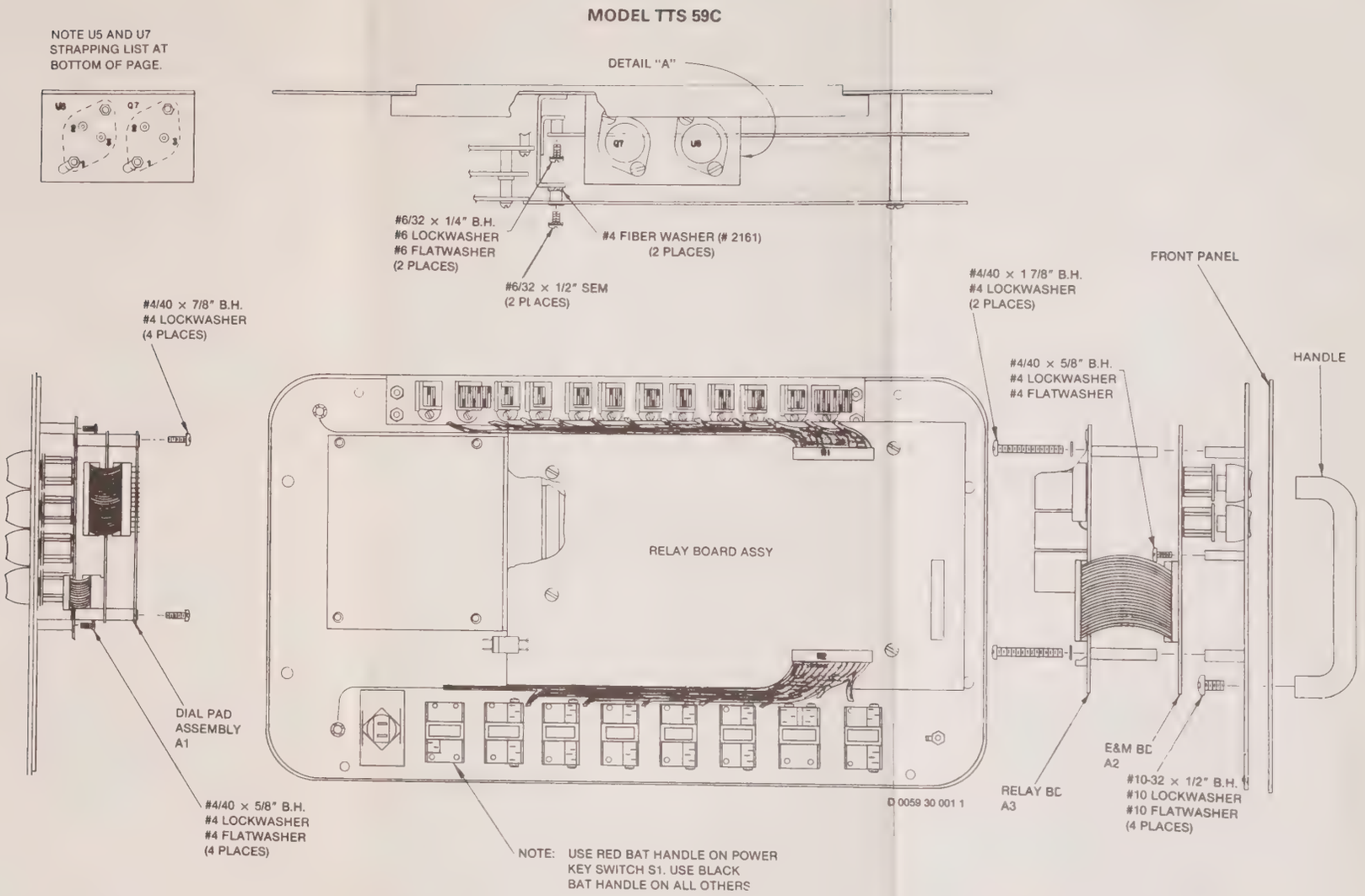


Figure 6—12. Model TTS 59C Interconnection Diagram.

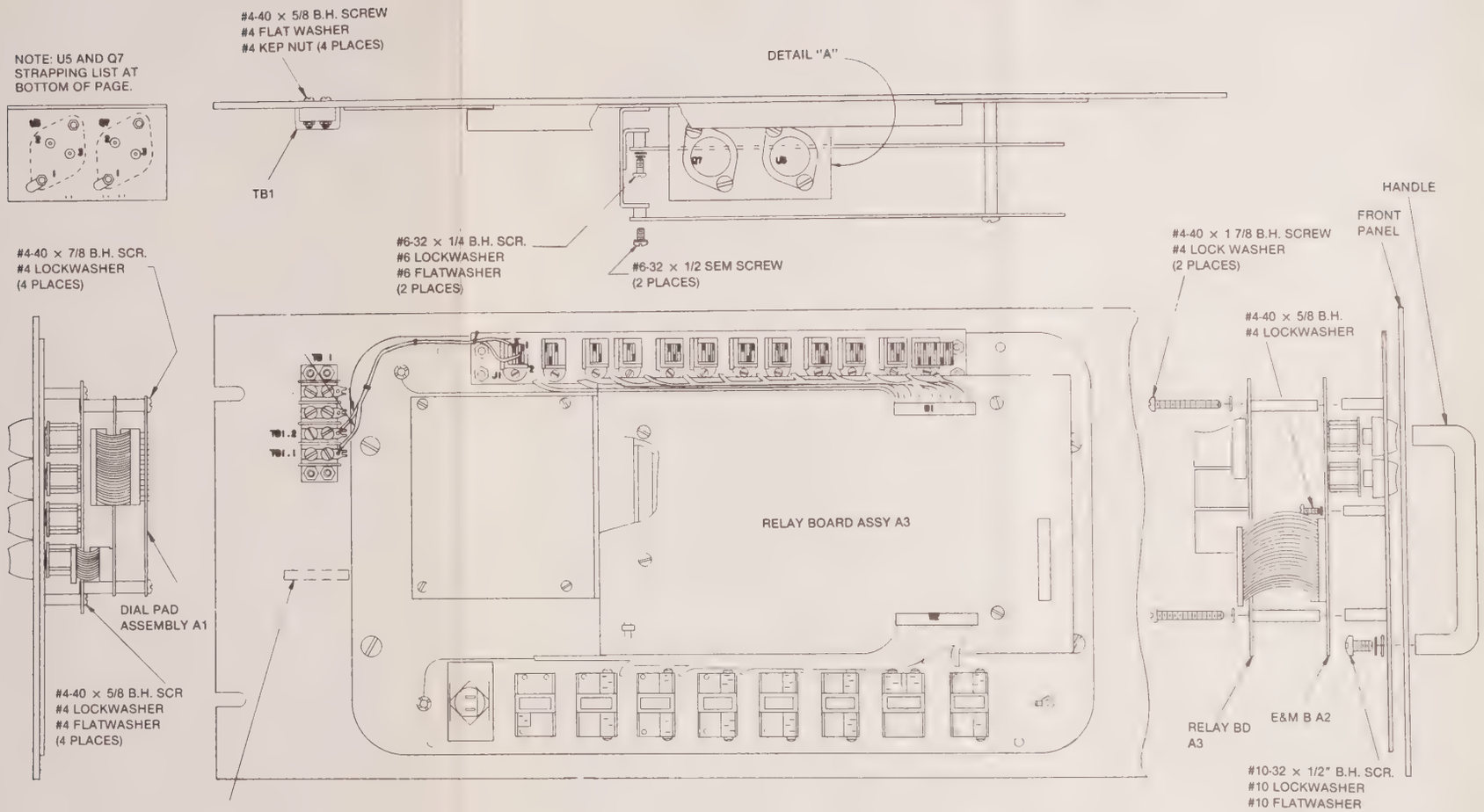


WIRING FROM U5 AND Q7

22 AWG	FROM	TO
STRAP	U5.1	U5.1 ON 0059-30-017 E&M BOARD
STRAP	U5.2	U5.2 ON 0059-30-017 E&M BOARD
STRAP	U5.3	U5.3 ON 0059-30-017 E&M BOARD
STRAP	Q7.1	Q7.1 ON 0059-30-017 E&M BOARD
STRAP	Q7.2	Q7.2 ON 0059-30-017 E&M BOARD
STRAP	Q7.3	Q7.3 ON 0059-30-017 E&M BOARD

Figure 6—13. Model TTS 59C/CR Overall Assembly Diagram. (Sheet 1 of 2)

MODEL TTS 59C



WIRING FOR U5 AND Q7

22 AWG	FROM	TO
STRAP	U5.1	U5.1 ON 0059-30-017 E&M BOARD
STRAP	U5.2	U5.2 ON 0059-30-017 E&M BOARD
STRAP	U5.3	U5.3 ON 0059-30-017 E&M BOARD
STRAP	Q7.1	Q7.1 ON 0059-30-017 E&M BOARD
STRAP	Q7.2	Q7.2 ON 0059-30-017 E&M BOARD
STRAP	Q7.3	Q7.3 ON 0059-30-017 E&M BOARD

Figure 6—13. Model TTS 59C/CR Overall Assembly Diagram. (Sheet 2 of 2)

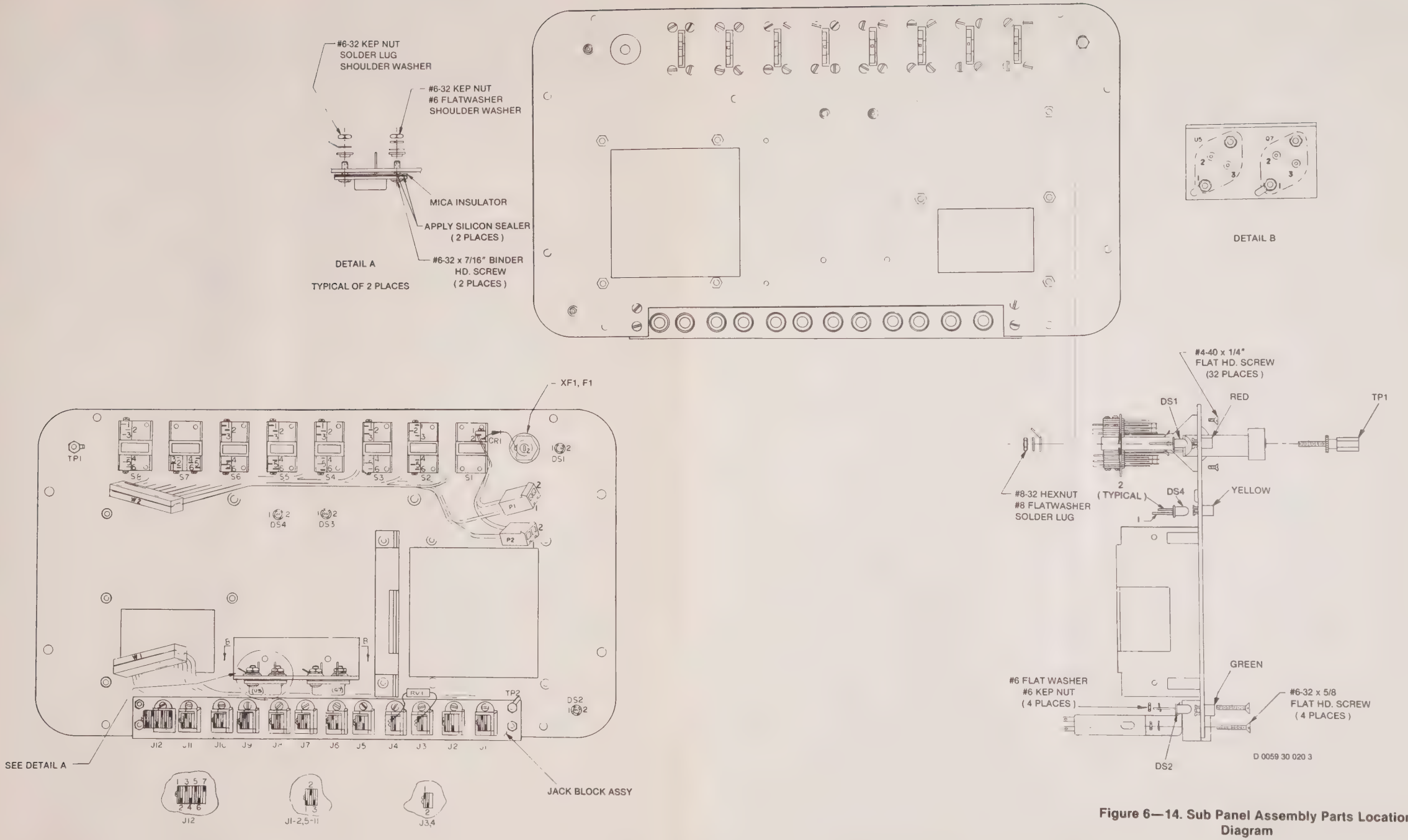


Figure 6—14. Sub Panel Assembly Parts Location Diagram

Figure 6—15. Jack Block Assembly

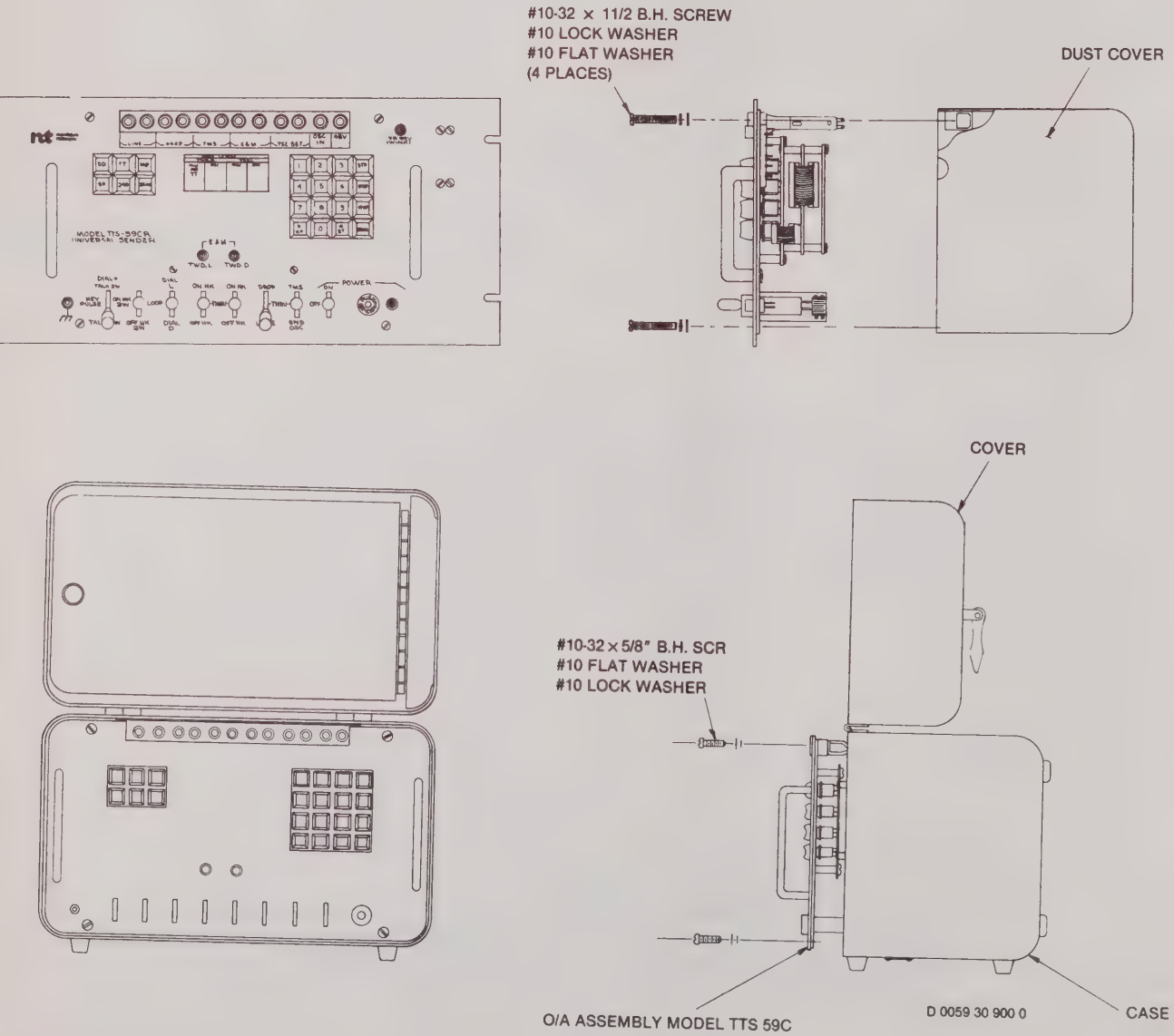


Figure 6—16. Model TTS 59C/CR Top Unit Assembly Diagram

SECTION 7

ELECTRONICS PARTS LIST

7.1 This section contains the electronics parts lists for the Model TTS 59C.

Table 7—1. Model TTS 59CR Overall Parts List.

N O R T H E A S T REPLACABLE PARTS LIST FOR ASSEMBLY C0059-30-019
E L E C T R O N I C S DIAL PAD ASSY PAGE 1 REV 05 DATED 5/23/80

REFERENCE DESIGNATOR	D E S C R I P T I O N VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
A1	PC ASSY 96910 SWITCH BD						A005930018
A2	DIAL PULSE BD ASSY						A005930023
A3	P.C. BD. 96887 TONE GEN.						A005930012

Table 7—2. Keypad A1 Parts List.

REFERENCE DESIGNATOR	D E S C R I P T I O N VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	PC ASSY 96910 SWITCH BD						A005930018
A2	PC ASSY 96888 DIAL PULSE						A400001014
A3	PC ASSY 96887 TONE GEN.						A400001015

Table 7—3. Dial Pulse Generator A1A2 Parts List.

N O R T H E A S T REPLACABLE PARTS LIST FOR ASSEMBLY C4000-01-014
E L E C T R O N I C S PC ASSY 96888 DIAL PULSE PAGE 1 REV 07 DATED 5/23/80

REFERENCE DESIGNATOR	D E S C R I P T I O N VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	.047UF		1%	100V	F-DYNE	PPT11-.047-100-1	322304731
C3-8	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C9	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C10-13	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C14	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C15	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1-3	D035 4NS 10MA		SI	50UA	FAIRCHILD	IN4148	560041480
J1	5 DIL				BERG	65610-110	654003331
J2	13 DIL				BERG	65610-126	654003323
K1-2	MERC.IMPREG,FORM 1A				MIDTEX	172-212SB7	604100012
L1	4 MH		2%		TRIAD	EM-004	460100001
Q1	TO-92 350MW TA		NPN	40V	MOTOROLA	2N3903	550039030
R1-8	4.7K	1/4W	10%		AB	TYPE CB	200104726
R9	330-	1/4W	10%		AB	TYPE CB	200103316
R11	4.7K	1/4W	10%		AB	TYPE CB	200104726
R12-16	100K	1/8W	10%		AB	TYPE BB	200001046
U1	16 DIP-P			CMOS	MOTOROLA	MC14409P	510004409
U2	18 DIP-P			CMOS	NATIONAL	74C922	510274922
U3	8DIP-P			DS	TI	SN75451BP	510075451
U3	24 DIP-P			MOS	SIGNETICS	CN0122	514100002
U4	16DIP-P	B		CMOS	MOTOROLA	MC14528	510004528
U5	14 DIP-P	B		CMOS	MOTOROLA	MC14584BCP	510004584
U6	14DIP-P	B		CMOS	RCA	CD4001	510004001
U7	14 DIP-P			LS	T.I ONLY	SN74LS124N	510974124
U7	24 DIP-P			MOS	SIGNETICS	CN0121	514100003
U8	14 DIP-P	B		CMOS	MOTOROLA	MC14081BCP	510004081
U9	16DIP-P	B/UB		CMOS	MOTOROLA	MC14490VP	510004490
Y1	CRYSTAL,2.00MHZ				CRYSTEK	HC-18U	919100012

Table 7—4. Tone Generator A1A3 Parts List.

N O R T H E A S T E L E C T R O N I C S

REPLACABLE PARTS LIST FOR ASSEMBLY 80059-30-012
P.C. BD. 96887 TONE GEN. PAGE 1 REV 04 DATED 5/29/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1	15UF		10%	10V	KEMET	T330A156K010AS	310001560
C2	6.8UF		10%	20V	KEMET	T330A685K020AS	310006850
C3	1.0UF ME	Y5V	20%	100V	ERIE	8141-100-651-105M	330801051
C4-5	1.0UF MD	Y5V	20%	50V	ERIE	8131-050-651-105M	330801050
C6	47PF		2%	500V	ELMENCO	CM04ED470GO	335404701
C7	150PF DB	N3300	10%	1KV	CENTRALAB	DD-151	330001510
C8-10	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
C11	15UF		10%	10V	KEMET	T330A156K010AS	310001560
C12	1000PF		2%	100V	ELMENCO	CM06DA102GO	335401020
CR1		1W	1%	6.2V	SCHAUER	SZ6.2	562000620
CR3-4	A1	300N 30M	SI	.1MA	TI	1N661	560006610
E1	PROTECTOR S/V GAS				SIEMENS	B1-C90/20	566009020
J1	13 DIL				BERG	65610-126	654003323
J2	16 DIP				BURNDY	DILB16P-108	820101100
R1	470-	1/4W	10%		AB	TYPE CB	200104716
R2	576-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257601
R3	52.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220252321
R4	511K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251131
R5	57.6K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220257621
R6	1500-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215011
R7	10-	1/4W	10%		AB	TYPE CB	200101006
R8	1500-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215011
R9-10	6980-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220269811
R11	301K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230131
T1	XFMR PC P600CT/600CT				MICROTRAN	VM14-FPB	400100900
U1	16 DIP-P	B		CMOS	MOTOROLA	MC14520	510004520
U2	14 DIP-P	B		CMOS	MOTOROLA	MC14584BCP	510004584
U3	24 DIP-P			MOS	SIGNETICS	CN0122	514100002
U4	24 DIP-P				INTEL	8253	514001405
U5-6	14DIP-P	B		CMOS	RCA	CD4024	510004024
U7	24 DIP-P			MOS	SIGNETICS	CN0121	514100003
U8	16 DIP-P				MOTOROLA	MC1408P8	510100202
U9	8PD1L	80MW		180V	NAT.SEMI	LM1458N	500001458
U10	14DIP-P	B/UB		CMOS	RCA	CD4025	510004025

Table 7—5. E&M Board A2 Parts List.

N O R T H E A S T E L E C T R O N I C S — REPLACABLE PARTS LIST FOR ASSEMBLY C0059-30-017
PC ASSY 96919 E&M BD — PAGE 1 REV 05 DATED 5/23/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1	20UF			50V	SPRAGUE	TE1305	300202061
C2	10UF			16V	SPRAGUE	TE1155	300201060
C3	20UF			50V	SPRAGUE	TE1305	300202061
CR1-6	D041	1A	SI	800V	EDAL	1N4006	560040060
CR7	A1EE	5W	5%	22V	MOTOROLA	IN53583	562053580
CR8-9	A1EE	5W	5%	14V	MOTOROLA	1N53513	562053512
CR10-11	A1	300N 30M	SI	.1MA	TI	1N661	560006610
CR13	A1	300N 30M	SI	.1MA	TI	1N661	560006610
J1-2	13 DIL				BERG	65610-126	654003323
J3	2 SIL	.045 SQ			MOLEX	09-75-1021/KK156 SER	654003501
K1-4	3K			48V	NIPPON	MR10-N19	600601250
Q1-3	TO-92	350MW TA	NPN	40V	MOTOROLA	2N3903	550039030
Q4	TO105	350MW TC	PNP	80V	FAIRCHILD	2N4356	552043560
R1	4.7K	1/4W	10%		AB	TYPE CB	200104726
R2	680-	1/4W	10%		AB	TYPE CB	200106816
R3	46.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246421
R4	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R5	4990-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249911
R6	392K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239231
R7	133K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213331
R8	29.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220229421
R9	16.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216221
R10	54.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220254921
R11	41.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220241221
R12	8250-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282511
R13	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R14-15	270-	1/4W	10%		AB	TYPE CB	200102716
R16	100K	1/4W	10%		AB	TYPE CB	200101046
R17	82.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282521
R18	47.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220247521
R19	46.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246421
R20	680-	1/4W	10%		AB	TYPE CB	200106816
R21-24	4.7K	1/4W	10%		AB	TYPE CB	200104726
R25	1.5K	3W	5%		W LEONARD	TYPE 3X	210301525
R26	4.7K	1/4W	10%		AB	TYPE CB	200104726
R27	330-	1/4W	10%		AB	TYPE CB	200103316
RT1	MINI GB-13A,9 PIN TUB.SKT				SYLVANIA	GB-19A	730100101
S1-6	KEYBD SW,ALT ACTION				C.P.CLARE	S872-20	635900550
S7-8	DIP SWITCH,10 POSITION				CTS	206-010	640001002
U1-2	8PDIP			36V	TI	LM311P(SN72311P)	500003111
U3	14DIP-P	B/UB		CMOS	RCA	CD4023	510004023
U4	TO-220			-15V	FAIRCHILD	UA7915UC	500079151

Table 7—6. Relay Board A3 Parts List.

N O R T H E A S T E L E C T R O N I C S — REPLACABLE PARTS LIST FOR ASSEMBLY C0059-30-016 PC ASSY 96918 RELAY BD — PAGE 1 REV 07 DATED 5/23/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-4	2UF			200V	F-DYNE	MPE11-2.0-200-10	301302050
C5	10UF		10%	25V	KEMET	T330C106K025A	310001061
C6	.1UF MC		Y5V 20%	50V	ERIE	8121-050-651-104M	330801040
C7-8	.1UF DO		Z5U 20%	500V	SPRAGUE	5GA-P10	330401040
C9	20UF			50V	SPRAGUE	TE1305	300202061
C10	2UF			200V	F-DYNE	MPE11-2.0-200-10	301302050
CR1-12	D041	1A	SI	800V	EDAL	1N4006	560040060
CR13-16	A1 300N 30M		SI	.1MA	TI	1N661	560006610
J1-3	13 DIL				BERG	65610-126	654003323
J4	2 SIL .045 SQ				MOLEX	09-75-1021/KK156 SER	654003501
K1-2	RELAY,1A-PC				MIDTEX	172112B00	604103500
K1-2				** NO FIXFLE **			604103501
K3	MERC.IMPREG,FORM 1A				MIDTEX	172-212SB7	604100012
K4-16	3K			48V	NIPPON	MR10-N19	600601250
Q1	TO-5	1W TA	NPN	40V	RCA	2N3053	550030530
R1	604-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260401
R2	324-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220232401
R3-4	357-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220235701
R5	196-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219601
R6-7	432	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243201
R8	665-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220266501
R9-10	232-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223201
R11-12	604-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260401
R13	330K	1/2W	10%		AB	TYPE EB	200203346
R14	270-	1/4W	10%		AB	TYPE CB	200102716
R15	1.2K	3W	10%		IRC	PW3	210301226
R16	270-	1/4W	10%		AB	TYPE CB	200102716
R17	22K	1/4W	10%		AB	TYPE CB	200102236
R18	47-	1/4W	10%		AB	TYPE CB	200104706
R19	33K	1/4W	10%		AB	TYPE CB	200103336
R20	270-	1/4W	10%		AB	TYPE CB	200102716
R21-23	1M	1/4W	10%		AB	TYPE CB	200101056
R21-23				** NO FIXFLE **			210001056
R24	100K	1/4W	10%		AB	TYPE CB	200101046
R25	1M	1/4W	10%		AB	TYPE CB	200101056
R25				** NO FIXFLE **			210001056
R26	100K	1/4W	10%		AB	TYPE CB	200101046
R27-29	27K	1/4W	10%		AB	TYPE CB	200102736
R30	100K	1/4W	10%		AB	TYPE CB	200101046
R31	47K	1/4W	10%		AB	TYPE CB	200104736
R32	75K	1/4W	5%		A.B	TYPE CB	200107535
R33-34	270-	1/4W	10%		AB	TYPE CB	200102716
R35-36	470K	1/4W	10%		AB	TYPE CB	200104746
T1-2	XFMR,AUDIO,P-25K S-600				MICROTRAN	VM3-M	400100801
T3	TALK COIL				CECO	CE-104A	450100100
T4	HOLD COIL				N.T.I.	A024-0145	450200202
U1	14DILP	570MW			NAT.SEMI	LM3900N	500003900

Table 7—7. Sub Panel Assembly Parts List.

N O R T H E A S T — REPLACABLE PARTS LIST FOR ASSEMBLY D0059-30-020
E L E C T R O N I C S — SUB PANEL ASSY — PAGE 1 REV 04 DATED 5/23/80

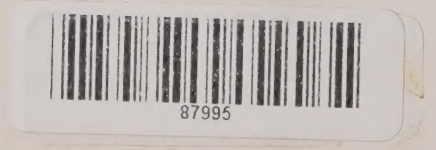
REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
CR1	D041	1A	SI	800V	EDAL	1N4006	560040060
DS1		10 MA			H.PACKARD	5082-4658	564500801
DS2	LED,HI EFF.GREEN				H.P.	5082-4958	564500807
DS3-4	LED,HI EFF.YELLOW				H.P.	5082-4558	564500806
F1		1A		250V	LITTELFUSE	3AG	863100400
P1	P1&P2 ASSEMBLIES						A005930007
P2	P1&P2 ASSEMBLIES						A005930007
Q7	TO3	87W	TA	PNP 80V	TI	2N4903	552049030
RV1	SILICON				SCHAUER	SV-1	565510000
S1	1A CONTACT				CAPITOL	1Z-14645-2156	630101201
S2-6	1D-1D CONTACTS				CAPITOL	1Z-14644-2166	630101303
S7	2D CONTACTS				CAPITOL	1Z-14643-2166	630101302
S8	1D-1D CONTACTS				CAPITOL	1Z-14644-2166	630101303
TP1	BINDING POST METAL GND				H H SMITH	137SP	652500100
U5	TO-3 20W(MAX)		5%	-5V	NAT SEMI	LM320KC	500003200
W1	W1 CABLE						A005930008
W2	W2 CABLE						A005930009
W2				** NO FIXFLE **			A00593009
XF1	FUSEHOLDER,3AG PANEL				BUSSMAN	HKP	863000100

Table 7—8. Jack Block Assembly Parts List.

N O R T H E A S T — REPLACABLE PARTS LIST FOR ASSEMBLY B0059-30-021
E L E C T R O N I C S — JACK BLOCK ASSY — PAGE 1 REV 00 DATED 5/23/80

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
J1-2	SPECIAL				SWCRFT	5J-1329	650401300
J3-4	SPECIAL				SWCRFT	5J-1194	650401200
J5-11	SPECIAL				SWCRFT	5J-1329	650401300
J12	JACK,TEL,SWCRFT SCHEM 22				SWCRFT	MT336C	650402200

39C



northern telecom

PRINTED IN U.S.A.

Northern Telecom Inc.
Northeast Electronics Division
P.O. Box 49
Concord, New Hampshire 03301

Tel. (603) 224-6511
TWX 710-361-1886
Telex 94-3453